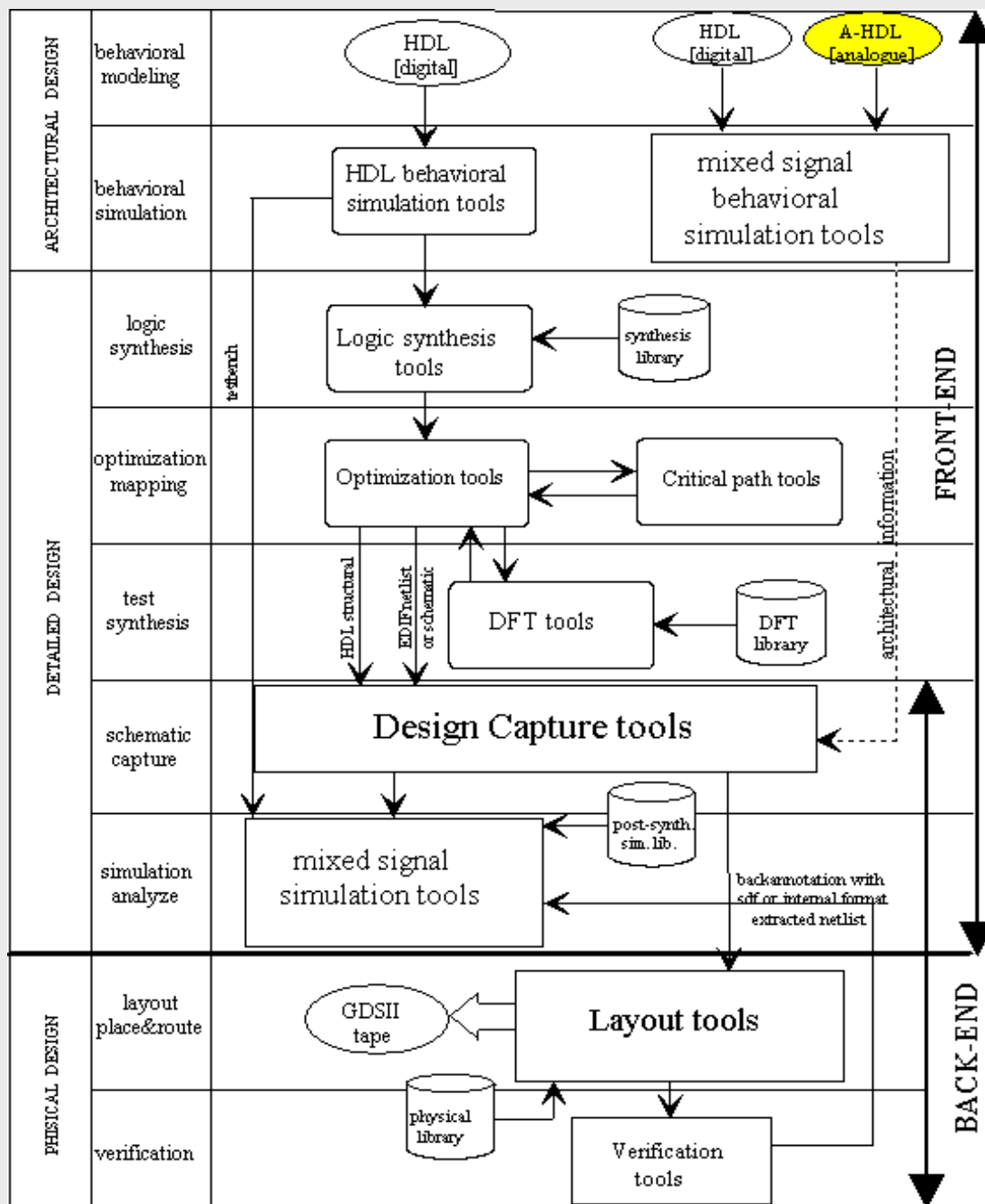
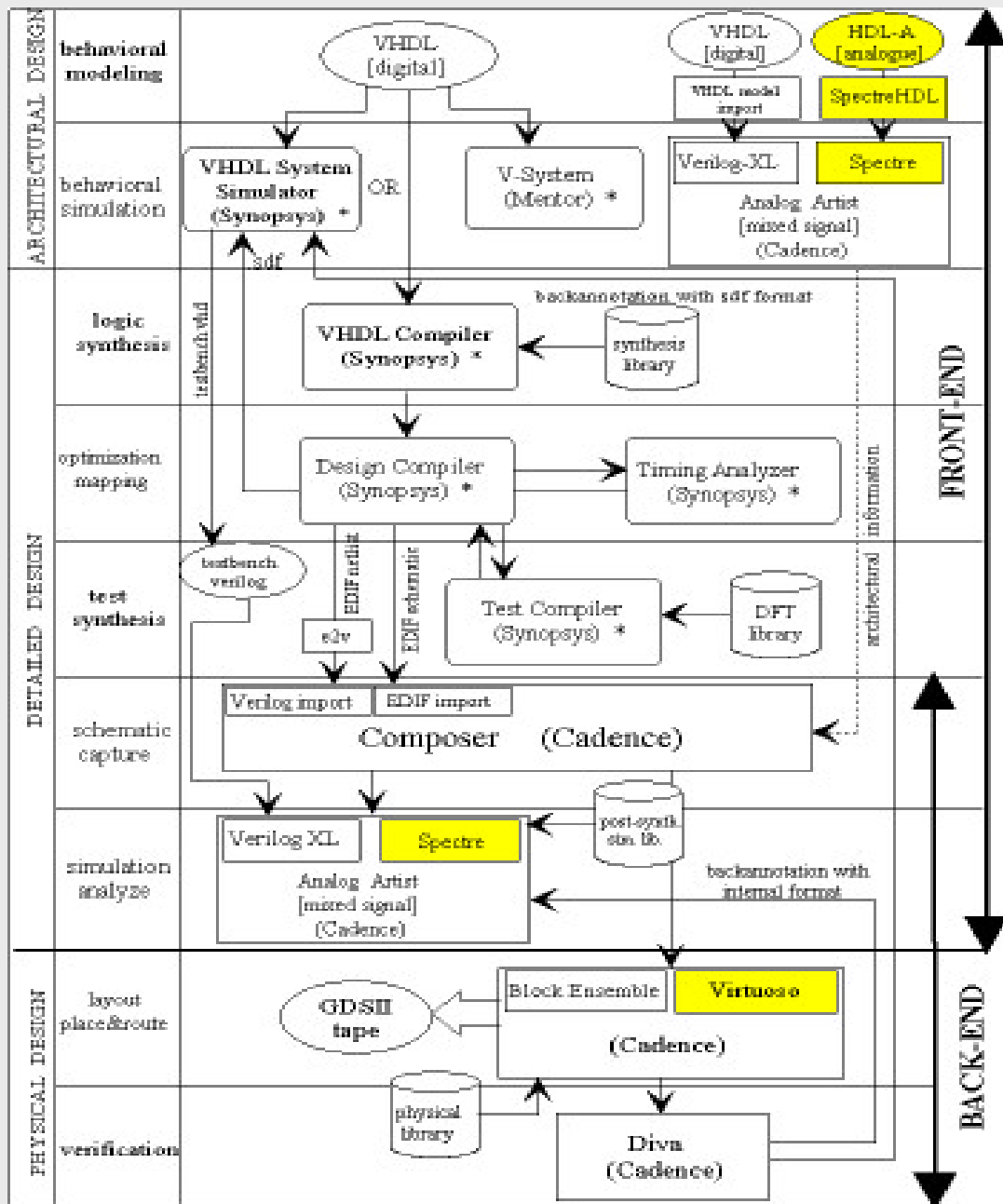


# MIXED SIGNAL ASIC DESIGN FLOW



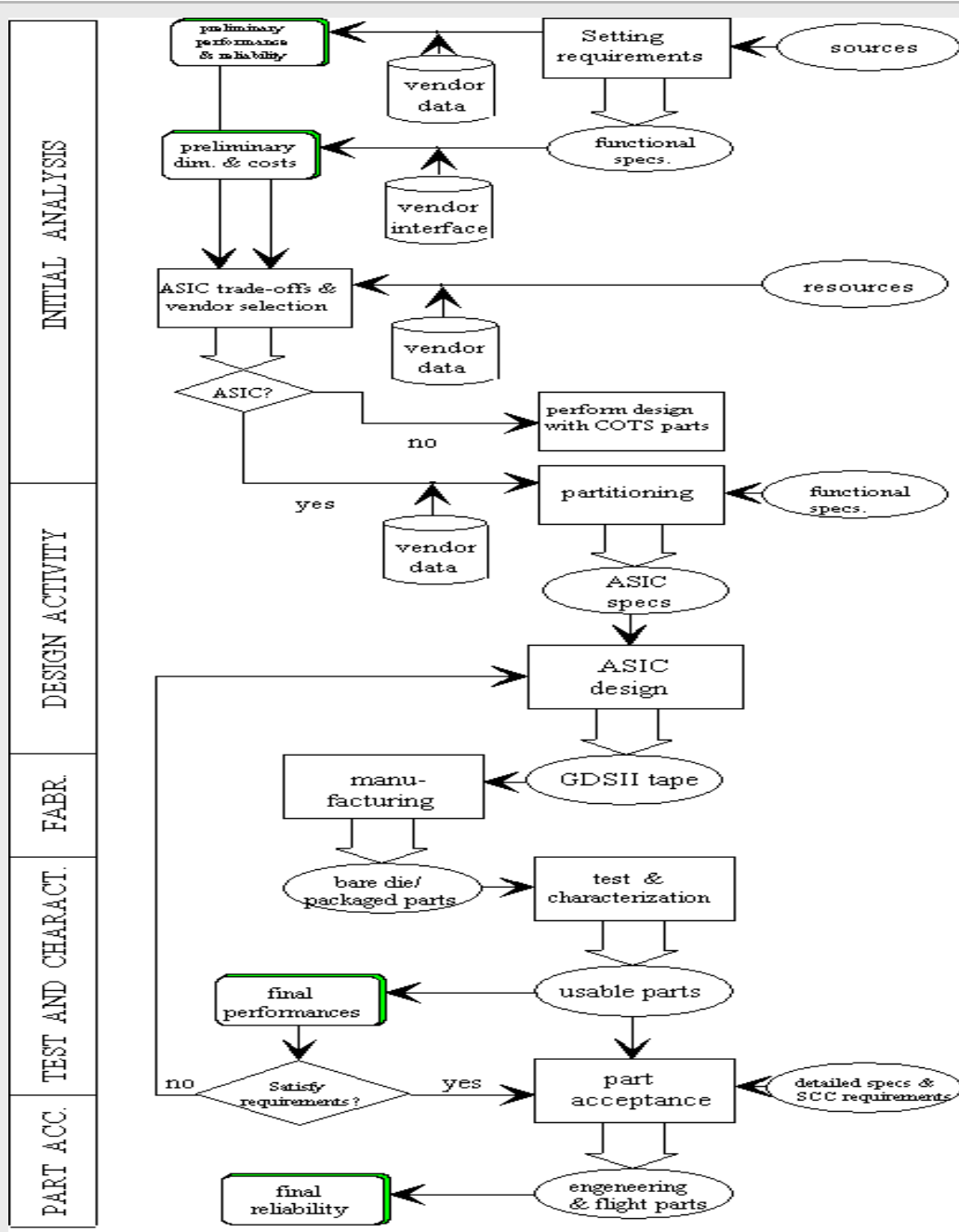
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# INTEGRATION WITH EXISTING CAD ENVIRONMENT



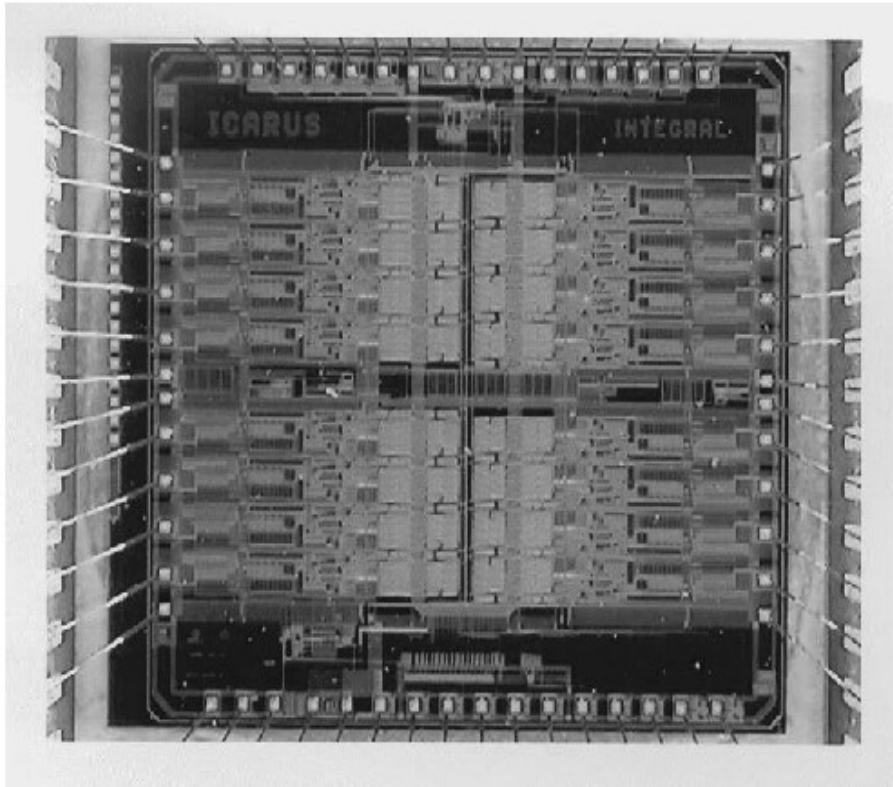
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# MIXED SIGNALS DEVELOPMENT FLOW FOR SPACE APPLICATIONS



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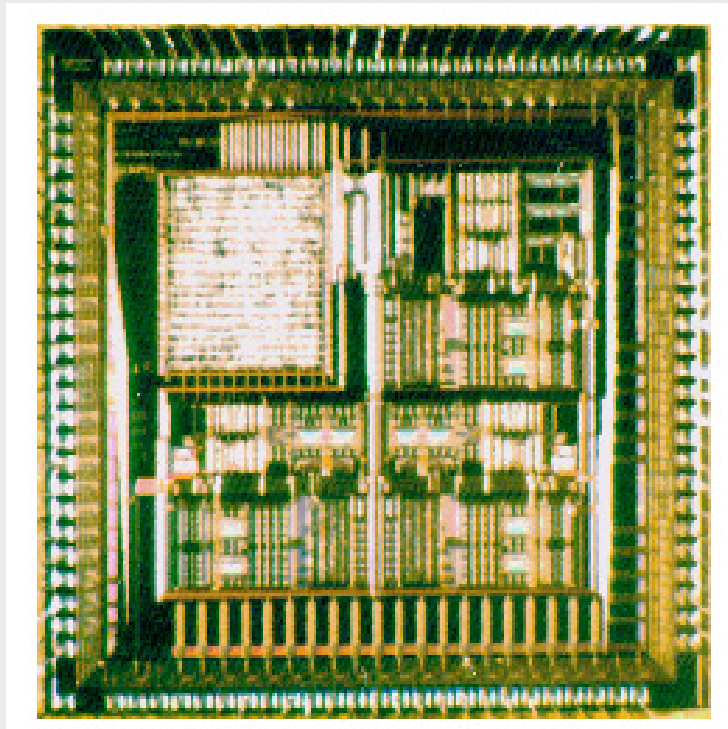
# ON FIELD APPLICATION *ICARUS CHIP MICROGRAPH*



Chip are including pads : 6 mm<sup>2</sup>.  
Package : 64 CQFP.

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ON FIELD APPLICATION  
*ABACUS CHIP MICROGRAPH*



Chip are including pads : 28 mm<sup>2</sup>.

N° of functional I/O : 98.

Package : 100 PGA.