

MIXED SIGNAL ASIC DESIGN METHODOLOGY FOR SPACE APPLICATIONS

L. Foglia, C. Ghidini, N. Ratti
LABEN S.p.A.
S.S. Padana Superiore 290, 20090 Vimodrone (MI) ITALY
Tel.: +39-02-250751 Fax: +39-02-2505515
E-mail: foglia.l@laben.it / ghidini.c@laben.it / ratti.n@laben.it

Prof. F. Maloberti, P. Malcovati
University of Pavia
Via Ferrata 1
I-27100 Pavia (Italy)
Tel. ++39-382-505205 Fax. ++39-382-505677
E-mail: franco@ele.unipv.it / piero@ele.unipv.it

ABSTRACT

ASIC products can provide system solutions that would not otherwise be possible with commercial off-the-shelf semiconductor devices. Reduction in system cost, volume and weight as well as increase in system performances are only few of the most obvious advantages. Sometimes, though, deciding to apply an ASIC design solution to an analogue or mixed-signal circuit can imply difficult decisions and trade-offs either in terms of technology and quality level offered on the market, or in terms of investments required to set-up a mixed-mode design environment and train enough resources.

This paper presents the results of studies performed at LABEN (a Finmeccanica Company), with the support of the Integrated Microcircuits Group of the University of Pavia acting as expert in analogue IC design, inherent to the introduction of a design methodology for the development of mixed signal (analogue and digital) ASICs for space applications aiming to broaden the digital ASIC standard design flow to the mixed-signal field.

The envisaged methodologies have been experienced in the development of two mixed-signal devices; in particular one development (e.g. ABACUS) is running in the frame of an ESPRIT project partially funded by EC.

1. INTRODUCTION

The increasing demand in miniaturisation and the high degree of reliability and quality that the electronic units for space application have to cope with, push to increase the “analogue content” within a single device (ASIC).

This holds true, for example, in the case of scientific instruments like IBIS, on board of INTEGRAL satellite, for which the entire front end electronic had to be integrated in mix-mode ASICs due to the extremely high number of detectors involved: only the PICsIT part of the experiment consists of eight modules each containing an array of 16 X 32 CsI(Tl) scintillators.

Moreover, personal communication satellites systems, smart sensors and also data handling subsystems are only few of the possible application area for mix-mode ASICs.

These competitive advantages that the capability to design and develop mix-mode ASICs can provide, must be supported by a set of accurate methodologies, either at management level or at operative level, that differ, in a lot of aspects, from purely digital ones, as it will be seen in the following.

The work presented in this paper, and started by LABEN since three years ago, has been divided into two main phases.

The former with the purpose to evaluate mixed signal ASIC technologies offered by the market and their associated foundries, the correspondent supported design tools and the qualification issues, with the final objective to identify a design flow and environment suitable for the technologies of interest, compatible with the in-house development system for digital ASIC, as well as recognised by the foundries as reference environment.

The latter with the purpose of defining a mixed signal ASIC development flow highlighting interfaces between subsequent phases, verification and control points as well as feedback and look-ahead points.

Finally the experience obtained on the field with the ABACUS project will be presented.

2. FOUNDRY SURVEY

Several key factors and evaluation parameters have to be considered in selecting a proper process and foundry, but most important is to establish a specific guideline for each different application. In fact every single parameter will have a different weight according to the application the ASIC product is meant for.

During this activity phase we identified a set of parameters to be analysed to assess suitability of a specific foundry and grouped them as follows :

General information on the process;
Packaging and testing facilities;
Qualification and radiation data;

Multi Project Wafer service;
Foundry interface.

In the following the evaluation parameters groups are explained in more details, giving particular emphasis to the problems concerning the space environment.

2.1. General information on the process

The selection of the proper technology needs to be performed verifying that the process can integrate the required functions in terms of speed, complexity and available cells. Furthermore for space applications it is very important to deal with a mature technology and a reliable process that offer low power consumption and good performances over a wide range of temperature and radiation.

To reduce the sensitivity of the process to radiation, the manufacturer can implement few enhancements modifying processing steps associated with oxide growth, since properly controlled oxide growth can increase total dose hardness, and using epitaxial, silicon-on-sapphire (SOS) or silicon-on-insulator (SOI) substrates.

These technologies have many important advantages for use in space applications: they exhibit improved latch-up immunity due to the epitaxial and insulator substrates and better radiation hardness over bulk CMOS. Furthermore reduced or no noise coupling exists through the substrate.

Unfortunately these processes are rather expensive due to the number of processing masks needed (even more than twenty) and their availability is somewhat limited.

2.2. Packaging and testing facilities

The capability of the manufacturer to perform packaging and mixed-signal testing activities for high reliability military and space systems has to be considered, otherwise a second source package manufacturer and test house need to be contacted.

Lately, also to provide a solution to packaging needs, designers are turning to MultiChip Modules (MCM) and Hybrids building the desired function up from ICs available in bare die form.

This has an impact on the selection of die with many factors needing to be considered:

- availability of suitable and tested die products;
- suppliers capability of meeting space level requirements;
- module level testing necessary to ensure reliability of the final system.

However it is important to consider that bare die test is very difficult to be performed and its cost increases exponentially the more the functionality that needs to be tested.

2.3. Qualification and radiation data

High-reliability space ASIC programs have stringent and unique requirements that not all ASIC vendors can meet.

In Europe a flight model ASIC needs to be manufactured according to the severe and stringent

ESA specifications documented in "Integrated Circuit, monolithic ESA / SCC Generic Specification N° 9000".

Unfortunately the qualification status as defined in the ESA document most of the time is not available especially in analogue fields, furthermore the foundries are not even interested in acquiring it because the procedure is too expensive and time-demanding and most of the times dedicated military product lines are even shut down.

On the other hand, among the standards that apply to ASICs, developed by the American Department of Defence, the MIL-I-38535 which refers to the Qualified Manufacturers List (QML) introduces a new concept. In fact under QML a manufacturer's entire fabrication process is qualified rather than the device types fabricated by that process. The implication of such an approach are that new products built on an existing line and using known design rules and production processes may be considered to have the same level of reliability as the other products from the line. In such cases the time required for the introduction of new products can be reduced significantly, since the main requirement becomes the characterisation of the product to determine its operating limits and not the qualification with lengthy periods of life testing.

2.4. Multi Project Wafer Service

The MPW (Multi Project Wafer) service enables companies to fabricate prototype ASICs at low cost by collecting designs from many users onto a single semiconductor wafer (MPW) thus sharing fabrication costs.

The service is offered by an EC initiative which aims to stimulate the wider exploitation of state-of-the-art microelectronics technologies by European industry: EUROPRACTICE.

EUROPRACTICE Basic Services will reduce the cost and risk for companies wishing to begin using new technologies.

2.5. Foundry interface

This issue is very important because an analogue designer, more than a digital one, should be able to seek information from the ASIC vendor who usually has a long-time previous experience on design problems related to the technology and their troubleshooting. It is not wise to switch vendors for small incremental gains, unless absolutely necessary, because users confront a steep learning curve for each vendor. This strict and close co-operation that needs to be developed between designers and production personnel is the main reason why particular emphasis was given to investigate European foundries with respect to world-wide available ones.

When vendors develop fabrication processes, library development naturally must follow the process developments the library aim to reflect. For example, to correctly extract all the necessary parameters to model a MOS transistor (for a BSIM3v3 model more than eighty are needed), the macrocell is implemented

in silicon on more wafers on different batches and with different geometries, verified for functionality and performance limits via actual hardware tests for different bias conditions and at different temperatures and finally the model values checked against measured device values. The vendor should maintain and control the design library with adequate configuration management including the following:

- cell library version control;
- cell library update control;
- trouble tracking reports;
- notification policy for major and minor changes to cells, related tools and related processes;
- current and complete documentation on the use and application of design cell libraries.

Related to foundry interface is the computer-aided design (CAD) tool issue. In fact mixed-signal ASIC projects require a complete set of CAD tools that map closely to a silicon vendor's entire flow and can support rather sophisticated analysis. Incompleteness, lack of proper integration, divergence from a vendor's flow or other inadequacies, like non certified design libraries, seriously endanger the success of an ASIC program.

ASIC vendors support a set of CAD tools that allow their customers to perform ASIC logic design and design verification with the vendor cell libraries. These tools must offer flexibility to support different choices of customer design approaches.

The evaluation of a vendor's supported tool set must show that the set can deliver all necessary design and design verification functions completely and in compliance with internal design methodologies, and that the vendor has adequate training programs and technical support available.

In the CAD evaluation job the following points are very important and should be verified:

- CAD tools offered by the ASIC vendor are either compatible with existing customer design tools, or upgradable with minimal impact on cost, time and training;
- design tools are all well integrated and have the capability to easily integrate new tools;
- the tools follow industry standards for design data and information exchange;
- the tools are largely diffused and supported by the main silicon vendors;
- the libraries developed for different tools are perfectly correspondent.

3. MIXED-SIGNAL ASIC DESIGN METHODOLOGY

In order to obtain a good level of quality in the integrated circuit design process, it is necessary to define a design methodology that identifies the set of activities to be accomplished and establishes a procedure with verification and control points. The main goals of any design methodology are to facilitate an optimum design along with the correct use of computer-aided design tools, to predict performances

and verify that they meet the specifications and, last but not least, to reduce design risks.

The approach of defining a design methodology should be adopted either when the design is being performed completely by a silicon vendor or solely by a system company or even jointly. In fact, in case one or more project phases will be subcontracted to third parties, it is important to accurately define the transition mechanism between a phase and the subsequent one and the required format of the interface media.

The work, performed at Laben, has identified a design flow that is as much general as possible, not bounded to specific design environment or technologies and that can assist both space and non space projects. The driving forces in the environment and tools selection were related to:

- identification of a simulator which is golden or reference simulator at several vendors that develop not only mixed-mode but also pure digital ASICs;
- availability of Design Kits supported by the identified development environment;
- availability of a reliable back-end tool, granting a safe backannotation process;
- integration with the existing environment.

In agreement to what just said, we visited few CAD vendor's facilities to get first-hand knowledge of their capabilities and tool-based design methodologies and we evaluated our proposed custom methodology, with respect to their specific tools, bringing a study case from Laben record. Main objective has been to determine a design flow with respect to new tools that will preserve previous tools introduced in Laben (e.g. Synopsys).

The evaluation work led to the identification of the design flow presented in figure 1, divided into two main phases mapped closely to the correspondent computer-aided design tools known as front-end and back-end tools.

The front-end tools are used for the following tasks: behavioral modelling, behavioral simulation, logic synthesis, optimisation mapping, test synthesis, schematic capture, simulation analysis.

The processes associated to the back-end tools are layout, place and route and verification.

The design approach has mainly been thought as a top-down one where the whole process, aimed to the development of the design from the highest to the lowest level, is divided into three main activities: Architectural Design, Detailed Design and Physical Design.

Each activity is itself divided into several steps, "minimised" in complexity, whose correctness is separately verified such that the problem of the conformity of the overall design with its specification can be guaranteed.

Each design step gives a particular view into the performance of the final device, the accuracy of which is dependent on the models used. It is obviously important the consistency between the models used at different levels of abstraction. Furthermore the use of library elements that are well characterised will contain design complexity problems and reduce design risks by

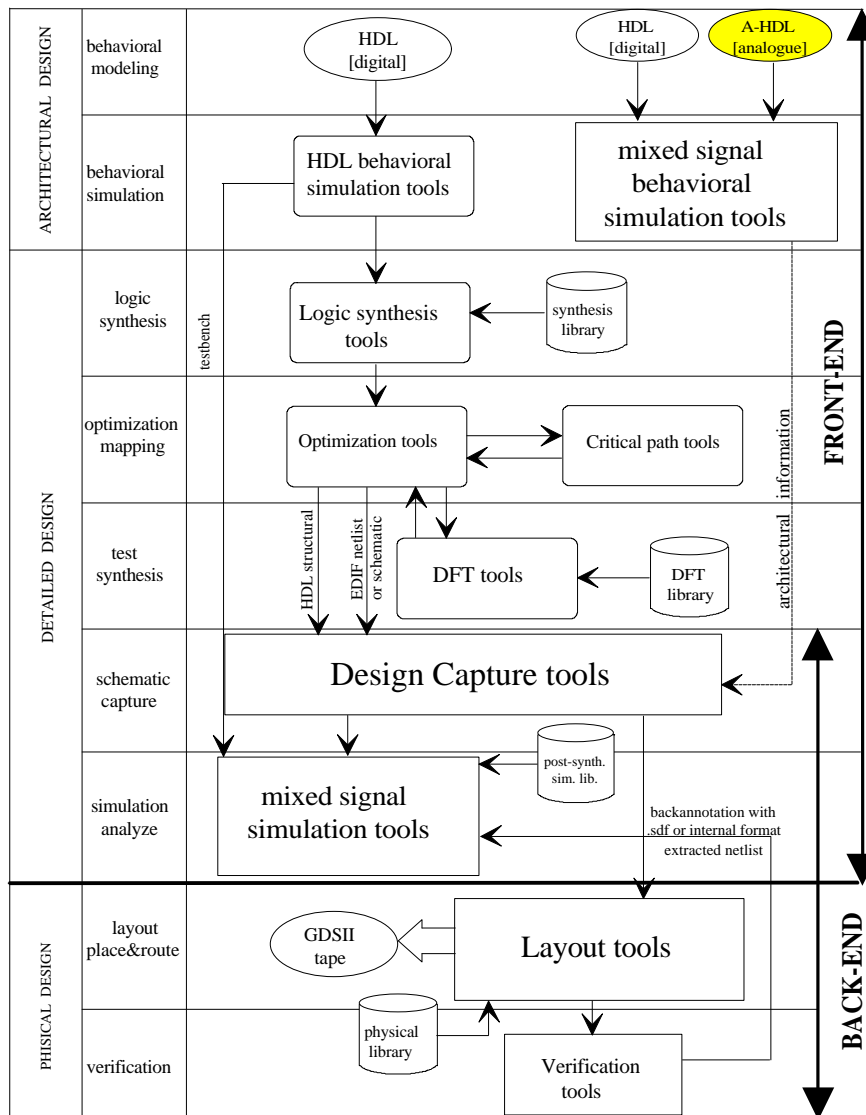


Figure 1: mixed-signal ASIC design flow.

modelling all important aspects of an ASIC's performance, including timing delays, post-layout capacitive effects, uncertainties due to process variations and performance variations due to changes in temperature and operating voltage.

In complex designs, the prediction of performances and their verification are not single steps, but multiple repetitions of a very disciplined set of comparisons realised on a hierarchical design either from the root down to its leaves (top-down approach) or from the leaves up to the root (bottom-up approach). Therefore, within specific activities the bottom-up approach can be utilised and still is the main one adopted for the analogue part of the design.

In fact, while for digital design a large and mature set of automated design tools exists for a top-down design methodology starting with a HDL-based high-level description (synthesis, optimisation, test and layout tools), the analogue designer is still using a schematic-based bottom-up methodology, thus mainly a manual

design, as it will be described in the following paragraphs dedicated to the three main design activities.

The Initial Analysis phase, whose output are the ASIC specifications needed to start the design work, will be described in the next section.

3.1. Architectural design

During this phase a behavioral description of the design is obtained. This mainly means that the preliminary idea of the design is evaluated and possible architectures compared, the design is functionally partitioned into its analogue and digital parts and subsequently large and complex blocks are decomposed in smaller and primary ones described in a Hardware Description Language (HDL: Verilog and VHDL for the digital part, Verilog-A and AHDL for the analogue part). This last step consists in clearly specifying the functions, interfaces and interactions of each block taking also into account the subsequent

implementation therefore transporting the ASIC specifications to the respective levels.

The HDL language is a very powerful mean at this stage since it allows a functional description of a design block without giving any insights on the possible implementation. This fact gives more than one advantage: in first place it allows the designer to start initial simulations, to evaluate different architectures, without spending time and efforts developing possible implementations which could be time consuming, especially for the analogue section where a transistor level design is mainly required. In second place for the digital section of the design, since the HDL language is the gate to automatic logic synthesis, it keeps the design technology independent so that it could be "re-targeted" to a different technology in a future.

As a matter of fact, a series of activities have been performed by the Open Verilog International (OVI) Analogue Technical Subcommittee to define the Verilog-A which follows the conventions and structures of the IEEE 1364 Verilog language, but is designed to simulate continuous-time and mostly-analogue systems. A follow-on phase to the Verilog-A initiative will be an OVI Verilog-MS language. Verilog-MS will be a superset of IEEE 1364 (digital) Verilog and OVI Verilog-A, and will be oriented towards complex mixed-signal "system in silicon" designs. On the other hand a correspondent VHDL Analog is under definition by IEEE 1076.1 working group.

With standardised languages though, meant to support top-down design methodologies for mixed-signal circuits, it will briefly be coming a shift, also for the analogue section of a design, from a schematic-based to a language-based methodology.

3.2. Detailed design

During this phase, gate-level submodule designs are performed for the selected process and library, strictly fulfilling the transported requirements of each sub-block.

At this point the digital and analogue design flows follow different methodologies: the digital an automated methodology while the analogue mainly a manual one.

The digital part of the design follows the consolidated standard design flow activities which will not be detailed for sake of conciseness: the VHDL models are automatically converted to gate-level description using the synthesis process with the support of the synthesis libraries, mapped to the target library and optimized for speed, area or power consumption. Static Timing Analysis is performed and one or more of the following approach implemented to increase the observability and controllability of the circuit: full or partial scan, JTAG (IEEE 1149.1), Built in Self Test (BIST).

A final electrical gate-level post-synthesis simulation is run with the support of the specific libraries to verify that functionality is still respected including the delays due to the single cells. Finally Automatic Test Pattern Generation (ATPG) is run to derive the test vectors that

fulfil the requirements for fault grading and toggle coverage.

On the other hand, the analogue section of the design needs to be schematically captured component by component from the appropriate library. This is a very delicate and time consuming task since most of the times the available building blocks are only transistors, unless a designer has been working on the same technology for a certain amount of time to allow a consistent proprietary library to be available. It relies on the designer's experience and capability to implement in the proper way what have been functionally taught and simulated. Different techniques (voltage feedback, switched capacitors, current feedback, switched current) need to be evaluated with respect to the requirements of the design in order to optimise it for speed, area, precision, noise immunity, insensitivity to power supply variations etc. Each analogue block is afterwards submitted to a very accurate analysis which comprehend the operating point, the DC and AC analysis, the transient and the noise analysis, verification of the performance after temperature and process variations.

Unfortunately no general fault models have been established for analogue circuits due to the fact that there are a much wider range of fault models in analogue circuits than in digital circuits therefore at the moment the common advice is to introduce, in the prototype runs of silicon, a certain number of test pins that allow the circuit to be monitored in appropriate nodes.

Finally once the digital and analogue sections of the design have been separately evaluated and processed, they are put together for final verification. This process is achieved thanks to a schematic capture procedure and a simulation backplane with automatic interface element generation for co-simulation of the analogue and digital part. Design requirements and compatibility with in-house existing tools dictate whether the design capture tools should have all or some of the following possible options:

- manual entry of netlist in a standard format such as Electronic Design Interchange Format (EDIF);
- symbolic entry;
- boolean equations or truth table entry;
- state diagram entry;
- HDL entry.

Mixed-signal modern simulators provide the capability of simulating various parts of a circuit using different modes (behavioral, logic, gate) simultaneously. This allows the designer to replace blocks of circuitry with behavioral models, that act exactly like the underlying transistors, once the function of those transistors has been verified. This fact gives the possibility to decrease simulation time dramatically.

Most of the times, simulation is carried out with a set of tests known as testbench, developed by the designer for the digital section and re-used with minor modification for mixed-mode simulation.

3.3. Physical design

The physical domain, in which the geometry of circuit elements and wiring connections are defined, represents the lowest and final domain in the design process. The physical design activity leads to the development of the layout of the integrated circuit which, in the appropriate format (GDSII), is then used for realising the photographic masks required in the chip fabrication.

For digital design, layout automation tools have been developed and are now commonly used with the relatively easy task to place the cells and route between them optimizing for area and signal delay. It's always a good advice, though, that the designer interactively participate to the automated process by making minor modification or taking direct control of critical cell blocks like fast circuitry and clock trees.

On the other hand analogue layout is strictly a manual activity performed with the support of a set of design rules, specific for each process. A skilled layout should be able to minimize the dependence of the simulated performances of the design from its physical implementation, thus mainly minimizing parasitic influences, crosstalk effects, temperature sensitivity and mismatch due to process inaccuracies. Typical techniques include minimization of junction capacitance in critical nodes by sharing junctions between transistors and minimizing junction perimeter and common-centroid layout to match errors caused by gradients effects in differential pairs thus reducing opamp input-offset voltage.

Furthermore when analogue and digital circuits are integrated onto the same chip, additional problems arise. The noise generated by the digital circuitry may couple into the analogue circuitry and corrupt the overall analogue circuit performance. Therefore, the control of the noisy interaction is vital in mixed circuits and can be done by careful circuit design (for example, by achieving good PSRR), but mostly it is more a matter of scrupulous layout. For example, the digital and analogue circuitry should be laid out in different sections of the chip, separated by guard rings and powered by different supply connections. Special care should go into the overall placement of different blocks (opamps, capacitors, switches, clock lines) of an analogue section containing switch-capacitors circuits. Finally the verification phase compares the circuit defined by a schematic diagram with that produced by a layout, verifies that a circuit layout conforms to the specification of the process technology design rules (Design Rule Check DRC), verifies the structure and integrity of a network (Electrical Rule Check ERC), performs device parameter measurement and parasitic device recognition and extraction.

These checks are automated and performed by the party involved in the layout activity.

The analysis of postlayout delays, for the digital part, is finally run and saved in standard delay format (SDF). These derived delays are "fed back" into the simulation models with a process known as backannotation, to verify that the requirements are still fulfilled.

Alternatively a so called extracted netlist can be derived from the physical database and simulated. This netlist contains more detailed information, with respect to the sdf file, about the resulting interconnect and parasitic loads. This procedure is usually used only for the analogue part since the extracted netlist for a several hundreds gates design can take even more than one day to be simulated.

4. MIXED-SIGNAL ASIC DEVELOPMENT FLOW

The development flow, presented in Figure 2, identifies the different activities (plain rectangular boxes) to be performed during an ASIC project plan, pointing out inputs and outputs from processes (circled entities), vendor data or support (cylindrical entities) and ASIC evaluation data (shadowed boxes). Though shown in a chronological sequence some activities require substantial look-ahead operations while some processes require multiple iterations for a single ASIC program, in particular for ASIC that contain a certain amount of analogue contents which can aim to first design success only 30% of the times. In fact, although the analogue circuitry, most of the times, constitutes only a small portion of the total chip area, it may be the limiting factor on overall system performance and the most difficult part of the IC design. This could be due to the fact that whereas digital design is relatively systematic, analogue design appears to be much more tricky and subtle and based on personal intuition. Another reason could be that while the digital basic cell can be "on" or "off" the analogue basic cell can work in many different points of its electrical characteristic, sometimes very difficult to predict because due to aspects like process variation or parasitic effects. This is way good library models represent a key starting point of a successful design.

The development process has been divided into four main phases: the initial analysis (setting requirements, ASIC trade-offs, vendor selection), the design activity (partitioning and ASIC implementation), the manufacturing process and finally the test and characterization process. If the components are delivered for flight use a further part acceptance activity needs to be performed to screen out devices that show serious potential problems.

During the initial analysis phase data are collected to be able to determine if it is convenient to develop an ASIC device for the specific application; the assessment of convenience is given, in this case, in terms of a trade-off between costs estimation, development times and achievable performances and dimensions.

Input to this preliminary phase is a collection of initial and generic user requirements about the system; for this reason this process should be carried on with all the partners such as users, system manager and designers.

The information do not need to be very specific but such to allow an identification of the system critical

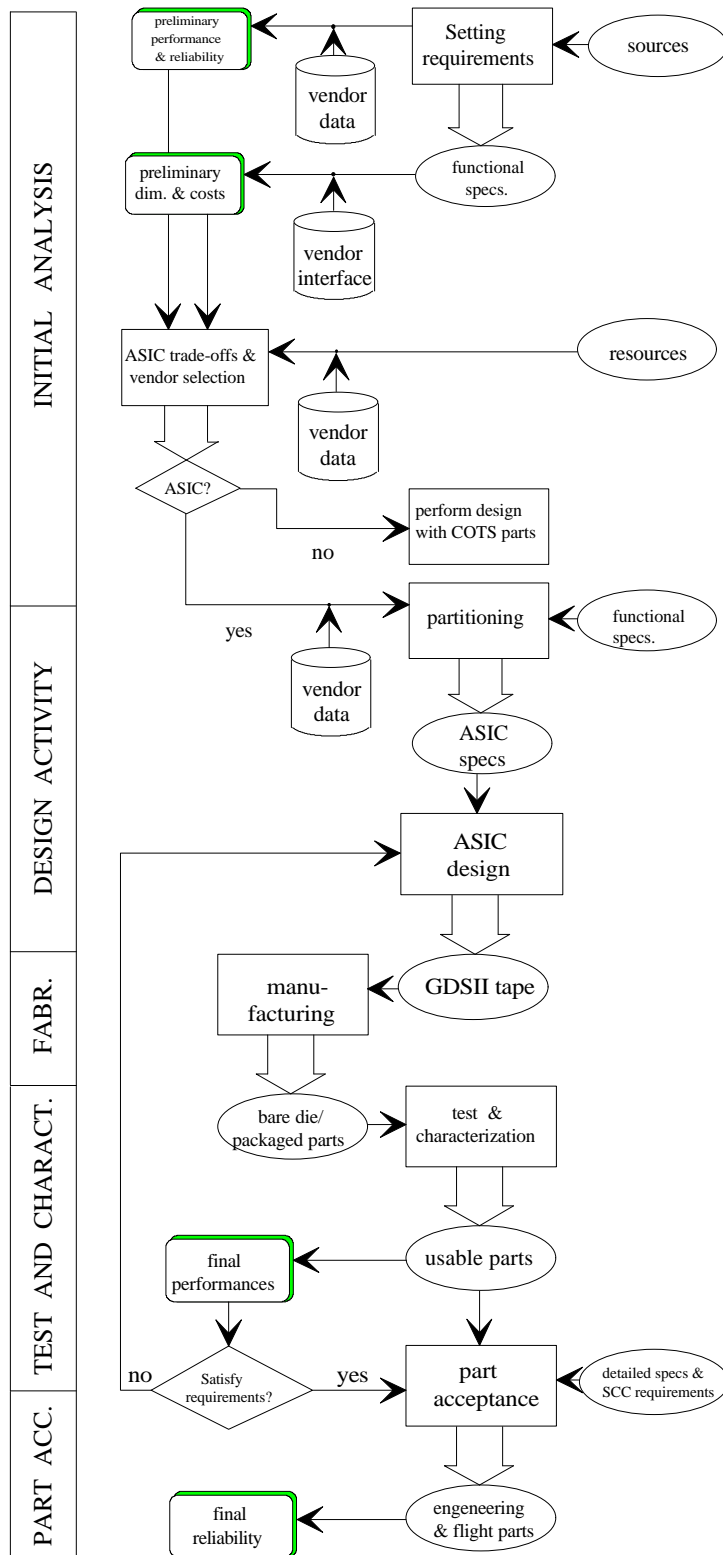


Figure 2: ASIC development flow

specifications and whether they will lead the design to limitations in terms of complexity and testability, operating frequency and packaging including the maximum number of input/output pins allowed and the achievable dimensions.

At this stage it is important to consider the

compromises and risks present in developing the chip in a given feature-sized technology from one vendor versus another feature-sized technology from a different vendor, the development tool available for the selected technology and the potentialities of these tools; the suitability, robustness and reliability of the

library together with the feasibility of all critical specifications in the selected technology.

The deeper the insight into the design and the functional specifications that come out from the previous considerations the less critical will be the task to predict preliminary dimensions and costs of the ASIC to be developed. This step is very difficult when dealing with full custom mixed-signal designs especially for what concerns the analogue part. Considerations about expected dimensions on the analogue part can be done with confidence only after a serious working experience on analogue layout in the target technology and obviously after the possible implementation has been thought.

During this phase the need to develop a module, part of a module or several modules in ASIC(s) shall be envisaged taking into account considerations about costs and packaging limitations and the compromises between miniaturising a critical section or implementing it with discrete components outside the ASIC device.

With the previous evaluation data at hand a management analysis should be carried on also considering the availability of engineering resources along with their experience and familiarity with the entire subject and the possibility to subcontract one or more activities to third parties.

If the results of this phase support the decision to develop an ASIC device, the design activities start with the ASIC specification phase during which all the detailed information deduced from the previous stages are formally documented. The importance of this activity is stressed even more when the ASIC design is not performed in house but procured from third parties. The ASIC specification, must be self-contained so that there shall be no need to consult other documents in order to understand what is to be implemented.

It is very important that the documentation is consistent and unambiguous which also pertains to same item having the same name through all documentation, and quality and performance parameters not leading to misunderstanding. As a consequence, parameters definitions, block diagrams, control flow charts, timing diagrams and other figures shall be introduced where beneficial for the understanding of the text. The reason for each requirement should be explained.

At this point the ASIC design activity starts and proceeds as described in the previous section having as final output the GDSII tape.

Before submitting the design for manufacturing, one or more meetings with experts from the foundry should be organized to review the design layout, especially of the analogue part, and receive general chip assembling technological suggestions.

Once the manufactured parts are delivered, when dealing with analogue devices, experimental characterization of prototypes is mainly performed in laboratory with classical instrumentation, like waveform generator and oscilloscope, making use of the test pins that were foreseen to detect internal nodes. This procedure is very delicate and completely different from the automated test of a pure digital ASIC;

sometimes it is very time-consuming and difficult to predict, definitely very important for successive optimization of the design. In fact, as already pointed out, while digital ASICs can aim to first design success, analogue designs need at least two silicon runs before going into production. During the first run a certain number of internal points are taken out (seriously increasing the pin-out count) to check for correctness and characterize the single blocks. If no major modifications are required, during a second run the final architecture of the design with the correct number of pins is developed, otherwise a third run is to be foreseen until the chip is fully functional within specifications.

Again when the production devices are to be screened out for flight use, analogue components encounter a more complicated procedure compared to digital ones since test equipment and electrical and functional measurements pre and post burn-in have to be thought "ad hoc" every time.

A consolidated analogue device screening does not exist and therefore a screening flow has to be defined and agreed with the final user every time.

5. ON FIELD APPLICATION

A possible application area for mixed-signal ASIC miniaturization was identified by Laben as the on board satellite bus system. In fact, in the last years, the increasing number of interconnected devices was pushing to the limit the electrical performances of the on-board data handling (OBDH) bus, producing significant signal distortion mainly because of the large load imposed. Therefore an evolution of the OBDH system, where huge RTUs are replaced by small integrated terminals (uRTUs), has been considered. Since with the presently available technologies it is indeed possible to realize miniaturized, low cost bus terminals, the single-chip ABACUS (Active Bus Adaptor and Controller for remote UnitS) becomes feasible. For the ABACUS design, in the frame of a joint European Design Cluster project between Laben, Micronova Sistemi and University of Pavia, we explored the potentialities of a new rad-hard full-custom BiCMOS SOI (0.8 μ m) technology developed by TEMIC and identified as DMILL. The DMILL technology sounded the most promising, among the processes investigated, in particular for its enhanced radiation performance. Furthermore, TEMIC participates to the EC initiative for Multi Project Wafer services EURO PRACTICE and offers the advantages of a QML line. However, since the technology is new, few difficulties arose in the design phase because of design libraries not consolidated. Finally, the design kit of the technology, developed only for the Cadence environment, lead to the acquisition of Cadence Design Framework II. The ABACUS circuit was designed by a mixed team, following the approach described in the previous sections. Therefore, after exploring the potential architectures and comprehending the requirements correctly, we assessed the final ASIC specifications and defined the final design architecture.

The ABACUS chip is fully functional and satisfies the specifications.

The identified development flow has been experimented in the design and development and qualification of the ICARUS Asic in the frame of the IBIS instrument on board of the Integral satellite.

6. CONCLUSIONS

In this paper we presented a design methodology and a development flow for the design and manufacturing of mixed mode asic for space application.

The paper highlighted the key factors that has to be taken into account for the introduction of a mixed mode asic design capability.

ACNOWLEDGMENTS

We recognize the support of F. Francesconi, M. Poletti, and S. Brigati from Micronova Sistemi for the helpful contribution in the development of the presented methodology.

References

- [RF 1] ESA, *ASIC Design and Manufacturing Requirements*, WDN/PS/700 Issue 2, October 1994.
- [RF 2] *Cadence reference manuals*, Cadence version 4.3.4 (95-02).
- [RF 3] Lectures of *DMILL seminar*, 4-5 February 1998, CERN Geneva Switzerland.

[RF 4] Eurocontrol DEI.3, *Requirements Development for the Tendering Process*, DASIA Proceedings 25-28 May 1998, Athene, Greece.

[RF 5] I.Millman, A.Gabel, *Microelectronics*, McGraw Hill.

[RF 6] R.S. Muller, T.I. Kaminis, *Device Electronics for Integrated Circuit*, John Wiley & Sons.

[RF 7] I.Fiez, *Analog VLSI: Signal and Information Processing*, McGraw Hill.

[RF 8] *ASIC Outlook 1997*, Integrated Circuit Engineering Corporation.

[RF 9] *The NASA ASIC Guide: Assuring ASICs for Space*, draft 0.6, 1993, Jet Propulsion Laboratory, California Institute of Technology.