

HIPADS - High-Performance Deep Submicron CMOS Analog-to-Digital ConverterS using Low-Noise Logic.



THE REDUCTION OF SWITCHING NOISE IN MIXED-SIGNAL DESIGN USING CURRENT STEERING LOGIC

Ecole Polytechnique Fédérale de Lausanne (CH-1015 Lausanne)

Mead Microelectronics SA (CH-1025 Saint-Sulpice)

ATMEL ES2 (F-13106 Rousset)

E_mail : kayal@epfl.ch

Outline

◆ Motivation

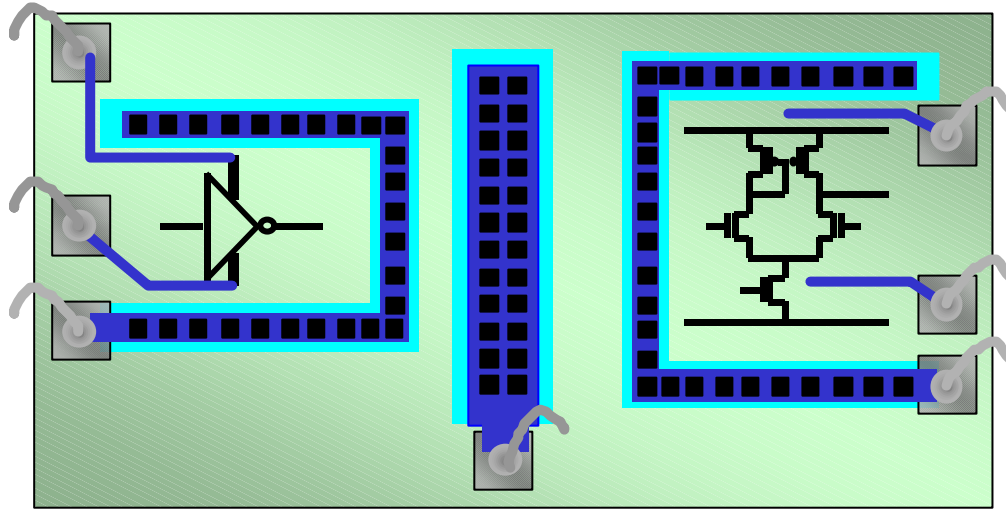
◆ Definitions

◆ CSL STUDY

- Theoretical study of CSL inverter based on G_v .
- Validation
- Theoretical study of FSCL inverter based on ξ .
- Validation.
- Comparison CSL x FSCL x Conventional static logic.
- Application

◆ Conclusions

Motivation - Solutions Used so far



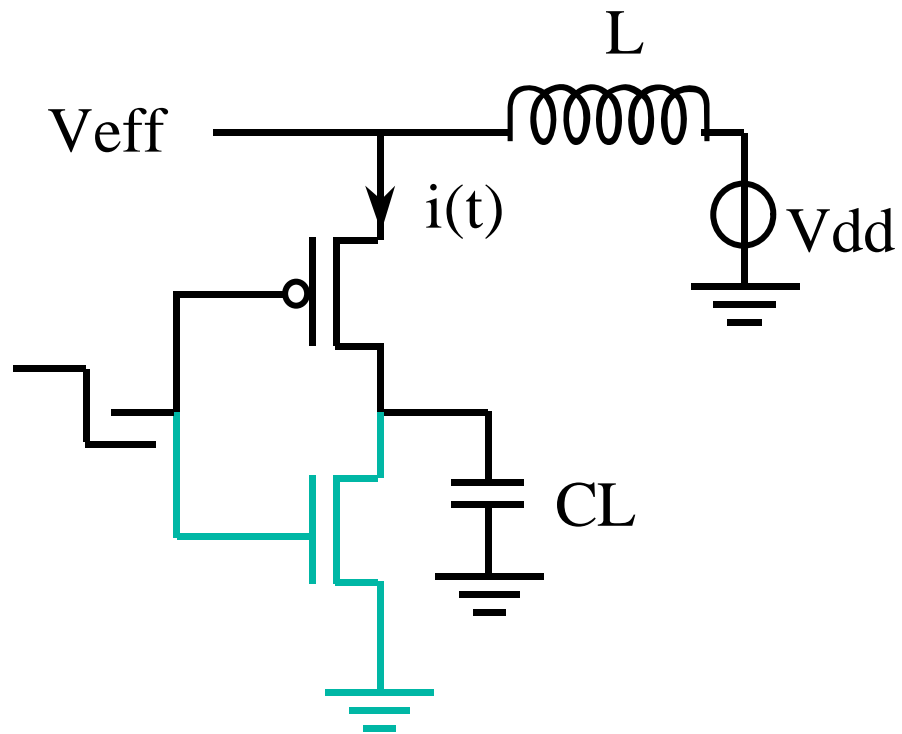
- ◆ Separation of digital and analog function.
- ◆ Shielding.
- ◆ Separation of power supply, grounds, bonding wires, etc.
- ◆ Contacts to the substrates with clean power supply lines (e.g. to avoid latch up).
- ◆ Fully differential analog circuits, low slew rate digital cells.
- ◆ Reductions of cross-talk

Motivation - Summary

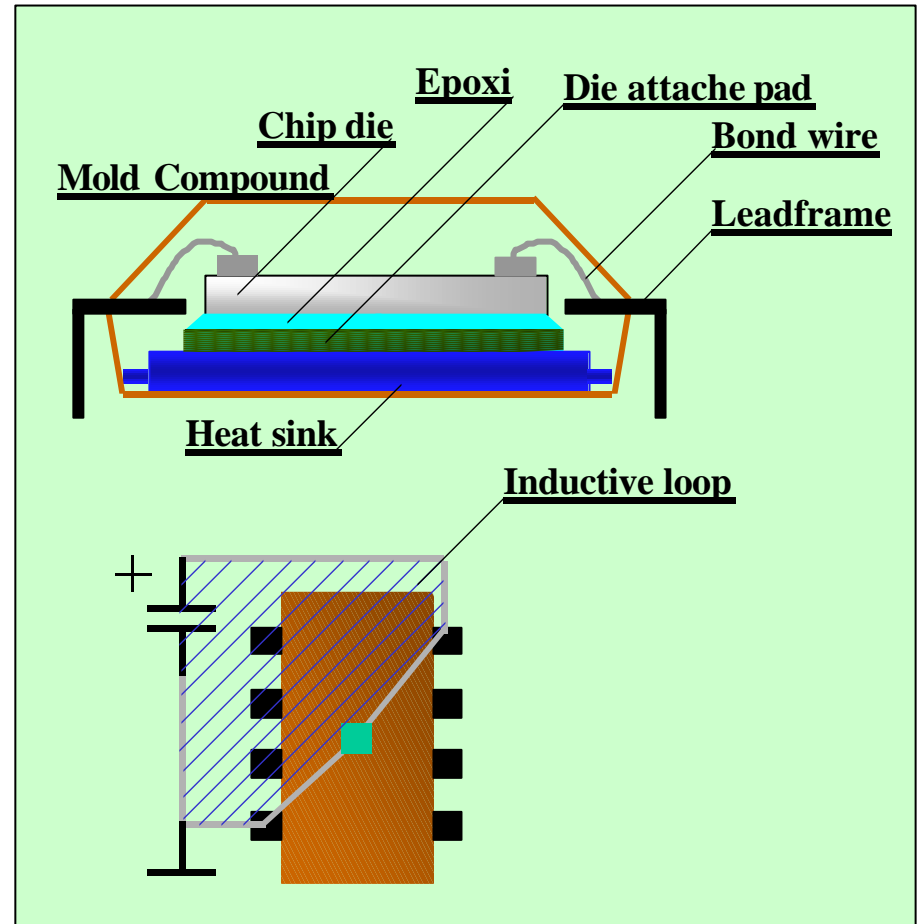
- ◆ Market issues - the reduction of price means reduction of the number of chips used in portable electronics, so we need mixed circuits.
- ◆ Technological issues - Tox requires reduction of power supply voltage.
- ◆ Mixed Analog/Digital circuit issues - They have to respond to the new aggressive design goals.

We propose to implement digital techniques that reduce the so called "digital switching noise", together with the entire arsenal of solutions used so far.

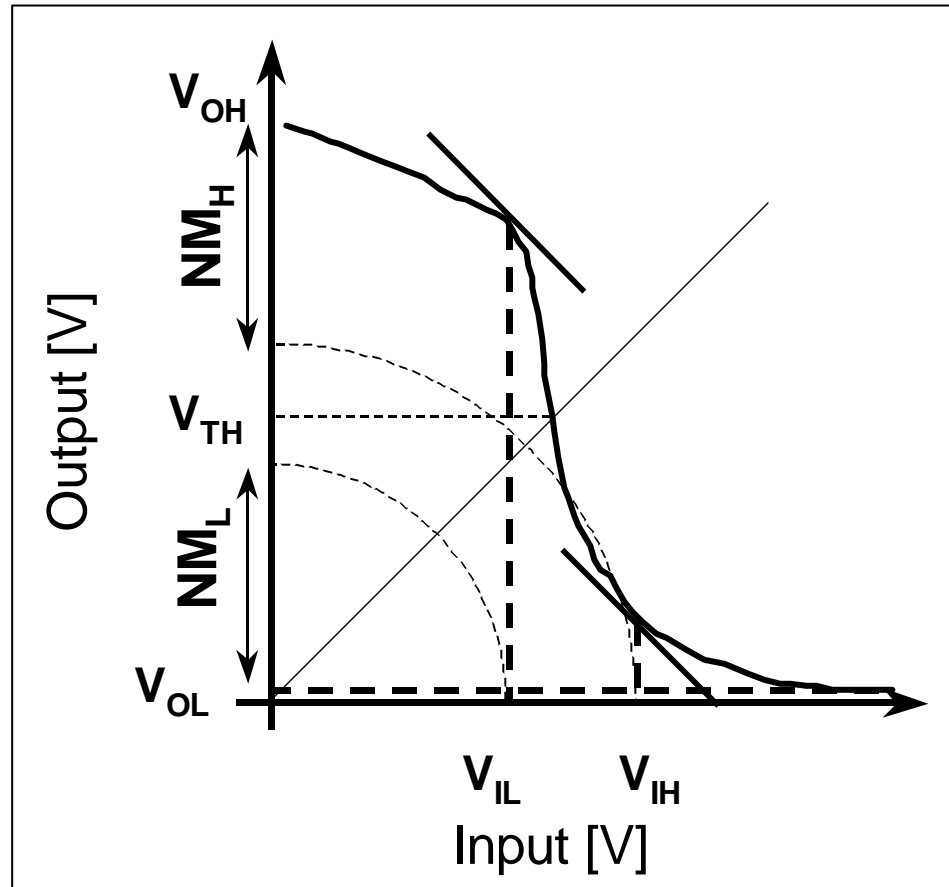
Definitions - Digital Switching Noise



$$V_{eff} = V_{dd} - L \frac{di(t)}{dt}$$

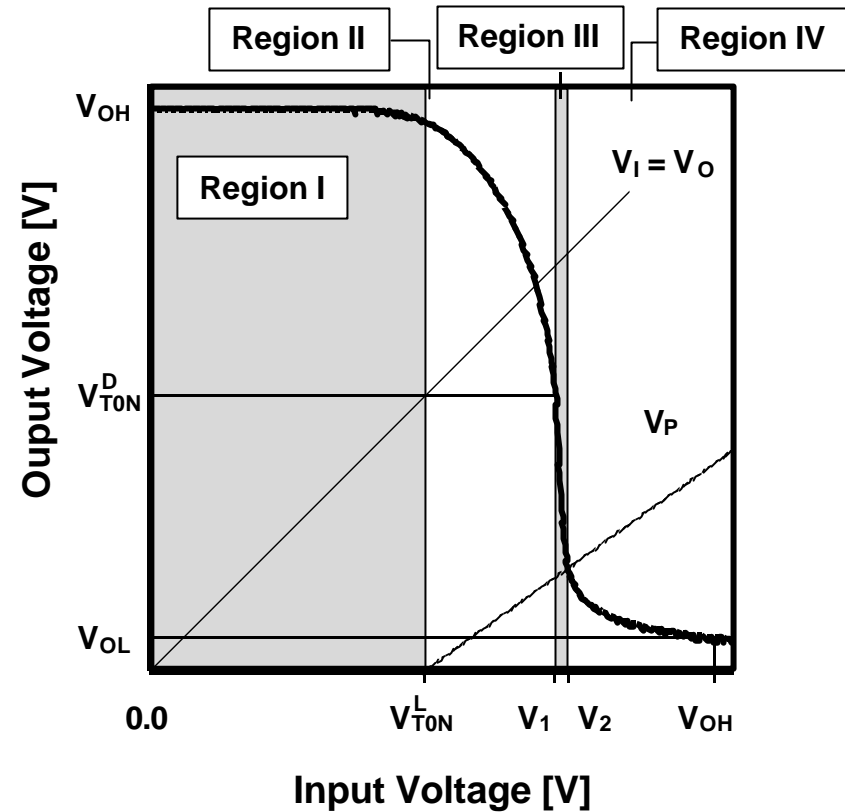
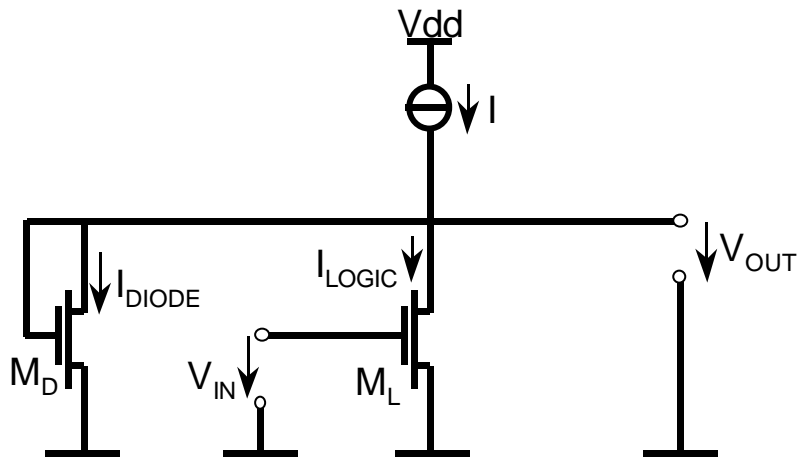


Definitions - Static Characteristics



Inverter Static Characteristics

Results - CSL Inverter Static Characteristics



◆ **G_v - parameter of design**

$$G_V = \frac{\beta_L}{\beta_D}$$

Region	M _L	M _D
I	OFF	ON - Saturation
II	ON - Saturation	ON - Saturation
III	ON - Saturation	OFF
IV	ON - Triode	OFF

Results - Static Characteristics Validation

- ◆ Output high logic level

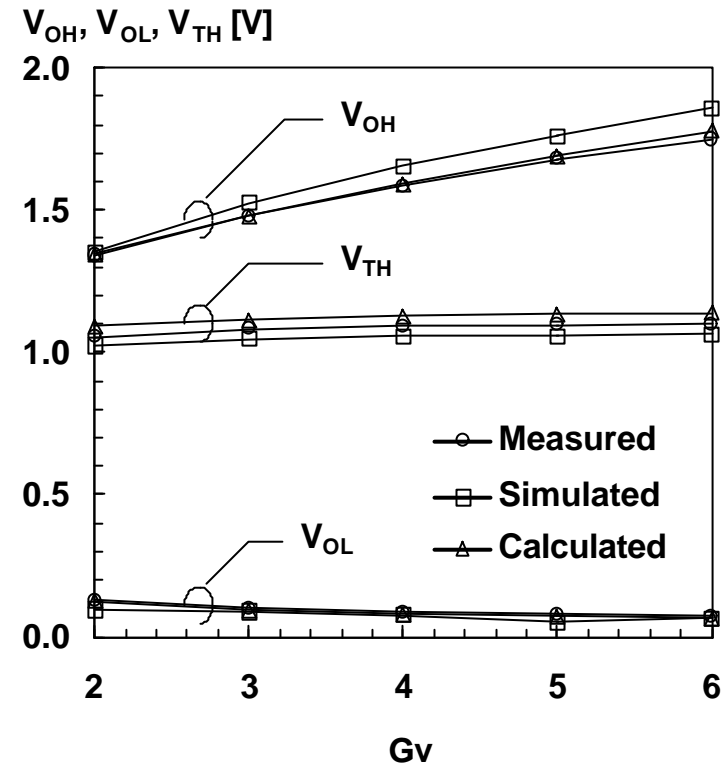
$$V_{OH} - V_{T0n}^D = \sqrt{\frac{2 \cdot n \cdot I \cdot Gv}{\beta_L}}$$

- ◆ Logic threshold voltage

$$V_{TH} = V_{T0n}^L + \left(\frac{V_{OH} - V_{T0n}^D}{\sqrt{1 + Gv}} \right)$$

- ◆ Output low logic level

$$V_{OL} = (V_{OH} - V_{T0n}^L) \cdot (1 - \sqrt{1 - Gv^{-1}})$$



The smaller the Gv the smaller can be the power supply voltage

Results - Static Characteristics Validation

◆ Low logic level noise margin

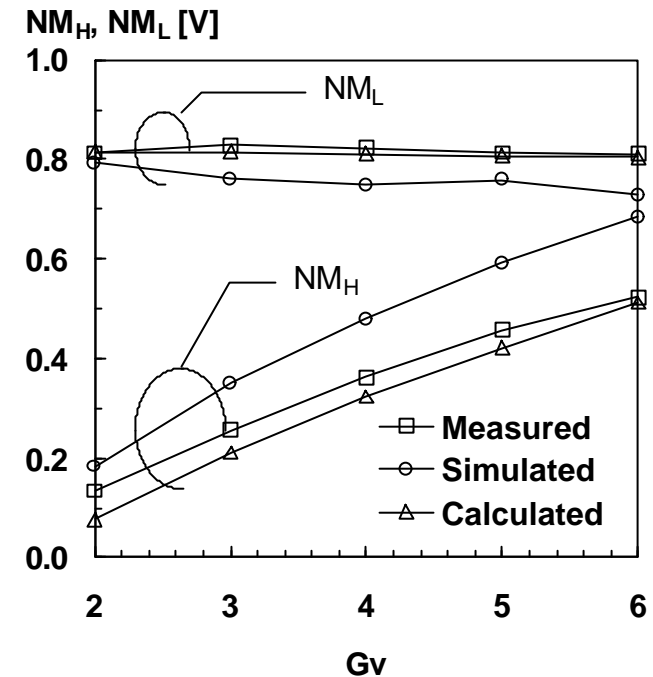
$$NM_L = (V_{OH} - V_{T0n}^D) \cdot (A - B) + V_{T0n}^L$$

$$A = \sqrt{\frac{1}{Gv}} \cdot \sqrt{\frac{1}{n^2 \cdot Gv + 1}}$$

$$B = \frac{1}{n} \cdot \left(1 - \sqrt{1 - Gv^{-1}}\right)$$

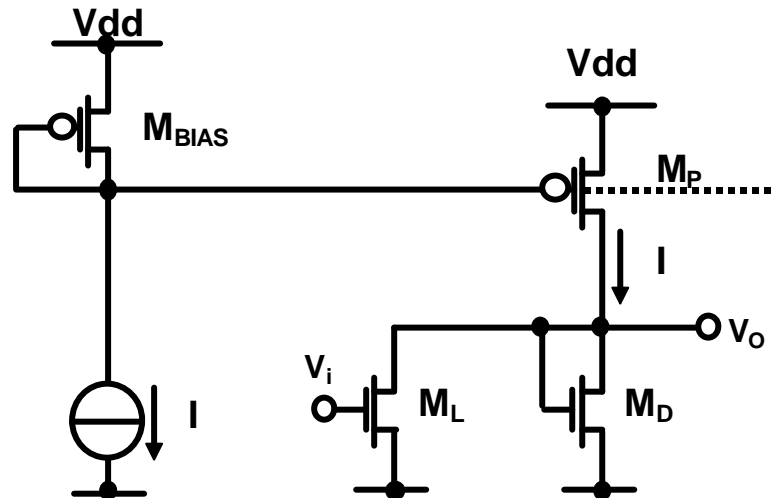
◆ High logic level noise margin

$$NM_H = (V_{OH} - V_{T0n}^D) \cdot \left(1 - \sqrt{\frac{(1+n)^2}{2 \cdot n + 1}} \cdot \sqrt{\frac{1}{Gv}}\right)$$

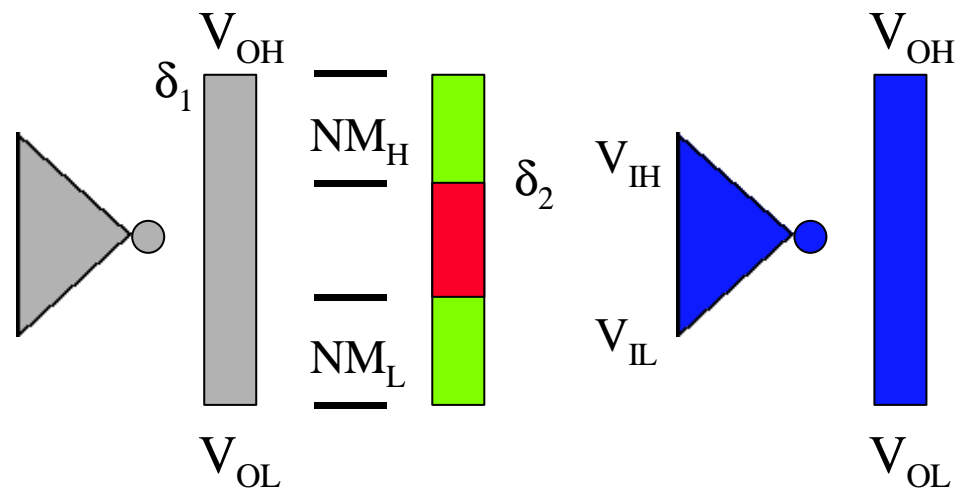


The higher is the Gv the large is NM_H , for a NM_L almost constant.

Results - Random Error Effects in CSL Inverter Noise Margin



- ◆ Mismatching characterized by δV_{T0} and $\delta\beta/\beta$.
- ◆ Non correlated V_{OH} and V_{IH} . They are characteristic of two different inverters, placed randomly on the chip.



Results - Second Order Analysis

- ◆ Variance of NM_H considering V_{OH} and V_{IH} non correlated

$$\begin{aligned} \sigma^2(\delta NM_H) = & \sigma^2(\delta V_{TON}^D) + \sigma^2(\delta V_{TON}^L) + \\ & \left(\frac{1}{2} \cdot \frac{n \cdot gm_P}{\beta_P} \cdot \sqrt{\frac{\beta_P}{\beta_L}} \right)^2 \cdot \left(\sigma^2\left(\frac{\delta\beta_P}{\beta_P}\right) + \sigma^2\left(\frac{\delta\beta_D}{\beta_D}\right) \right) + \\ & \left(\frac{1}{2} \cdot \sqrt{\frac{(1+n)^2}{2 \cdot n + 1}} \cdot \frac{n \cdot gm_P}{\beta_P} \cdot \sqrt{\frac{\beta_P}{\beta_L}} \right)^2 \cdot \left(\sigma^2\left(\frac{\delta\beta_P}{\beta_P}\right) + \sigma^2\left(\frac{\delta\beta_L}{\beta_L}\right) \right) + \\ & \sigma^2(\delta V_{TOP}^P) \cdot \left(\frac{gm_P}{I_P} \cdot \sqrt{\frac{\beta_P}{\beta_D}} \right)^2 \cdot \left(\frac{(1+n)^2}{2 \cdot n + 1} + \left(\frac{1}{2} \cdot \frac{n \cdot gm_P}{\beta_P} \right)^2 \right) \end{aligned}$$

- ◆ Example of application

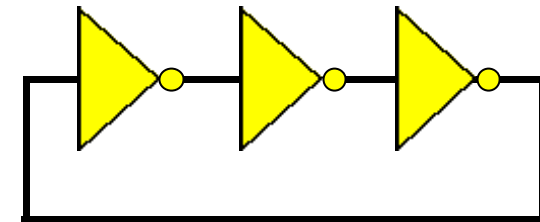
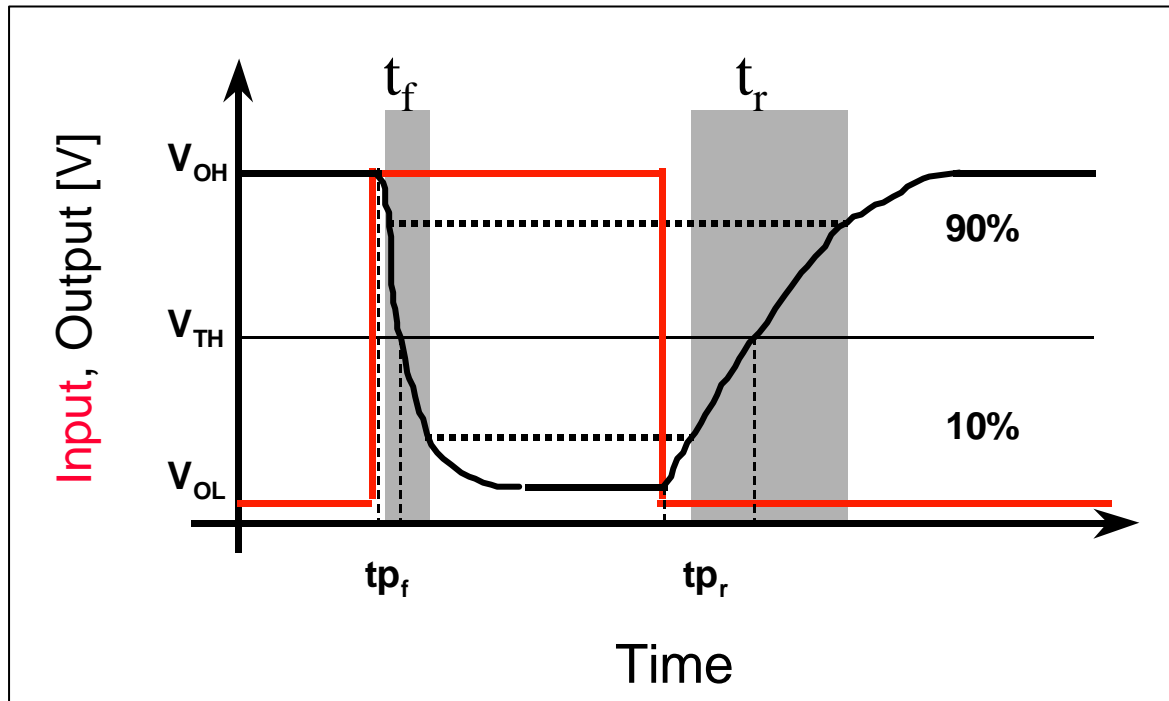
- $I=20 \cdot 10^{-6}$ A,
- $(W/L)_D=2.5\mu m/3\mu m$,
- $(W/L)_L=2.5\mu m/1\mu m$,
- $(W/L)_P=8\mu m/1\mu m$

Device	$\sigma(\delta V_T)$ [mV]	$\sigma(\delta\beta/\beta)$ [%]
M_D	~11	~1
M_L	~21	~2
M_R	~11	~1

$$\sigma(\delta NM_H) = 0.066V$$

The final noise margin should be positive.

Definitions - Dynamic Characteristics



$$tp = \frac{tp_f + tp_r}{2}$$

$$f_{os} = \frac{1}{2tp}$$

t_f - fall time

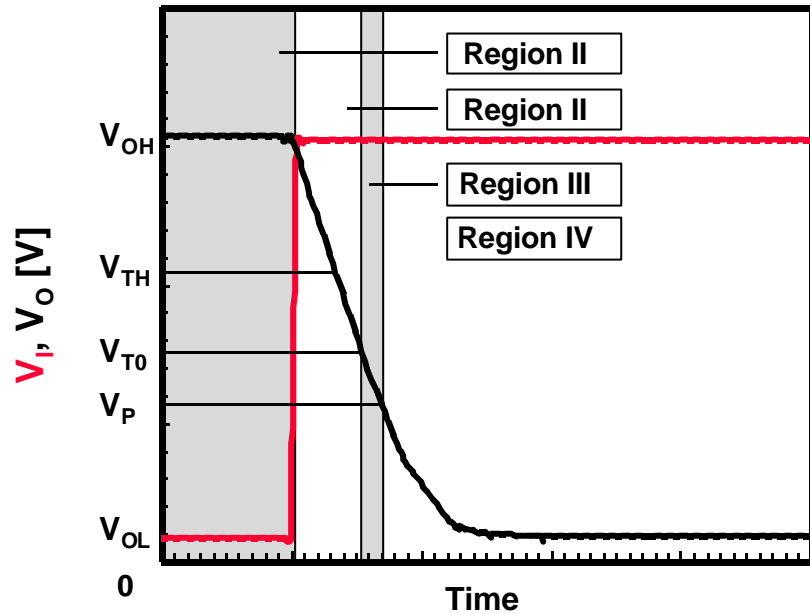
tp_f - fall propagation time

t_r - rise time

tp_r - rise propagation time

The input signal applied (red curve) is a step.

Results - CSL Dynamic Characteristics



Region	M_A	M_D
I	OFF	ON- Saturation
II	ON - Saturation	ON- Saturation
III	ON - Saturation	OFF
IV	ON- Triode	OFF

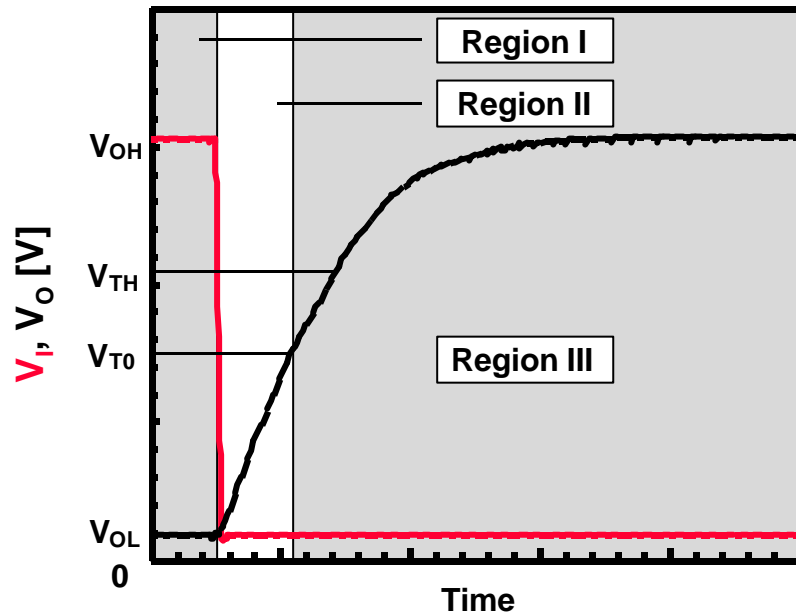
- ◆ High to low propagation time

$$t_{p_{HL}} = - \frac{\frac{2 \cdot n \cdot CL}{\beta_D}}{\sqrt{\frac{2 \cdot n \cdot I}{\beta_D} \cdot \sqrt{Gv - 1}}} \cdot \{A - B\}$$

$$A = \arctg \left[\frac{1}{\sqrt{(Gv)^2 - 1}} \right]$$

$$B = \arctg \left[\frac{1}{\sqrt{Gv - 1}} \right]$$

Results - CSL Dynamic Characteristics



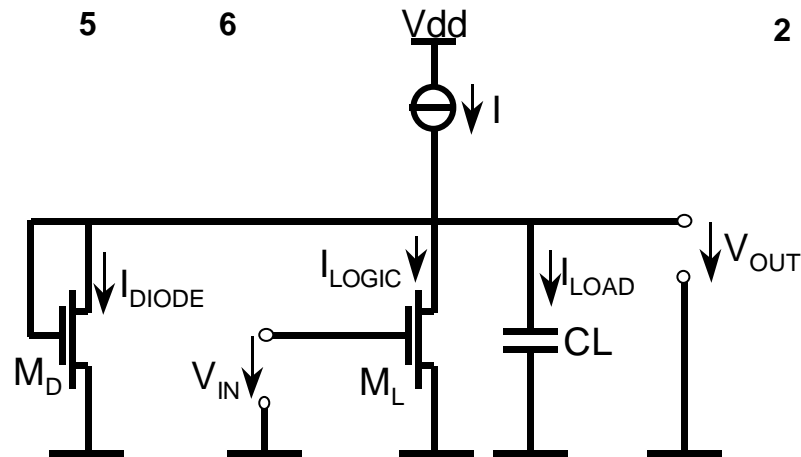
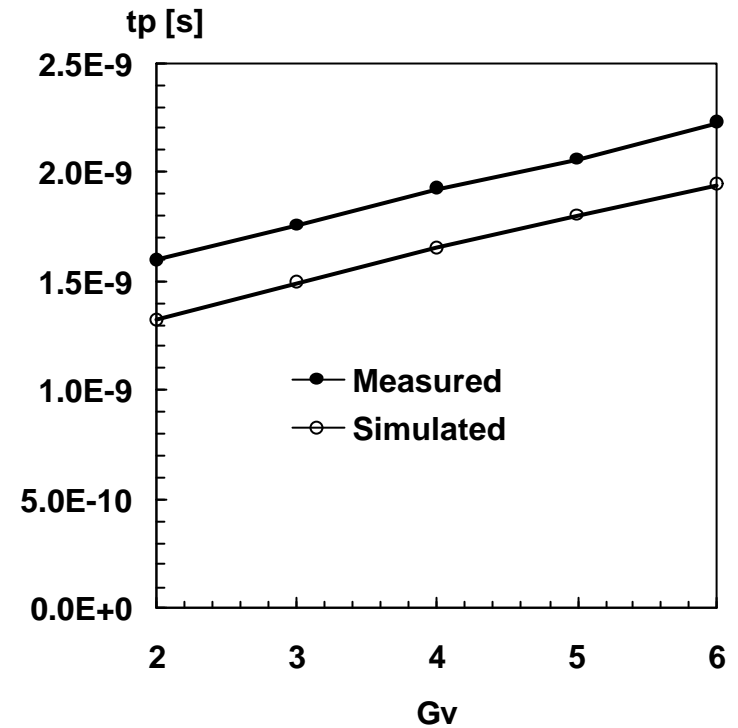
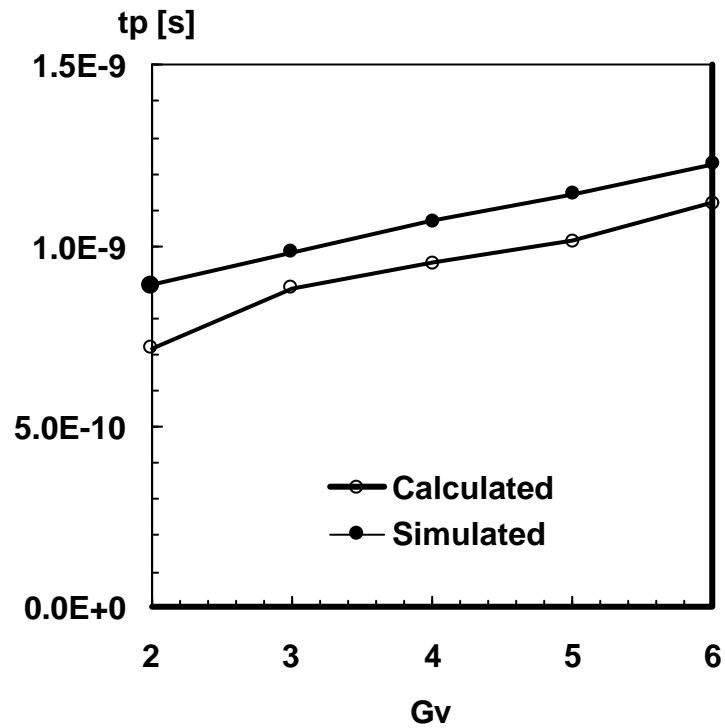
◆ Low to high propagation time

$$t_{p_{LH}} = \frac{CL}{I} \cdot (V_{T0n}^D - V_{OL}) + \frac{CL}{\beta_D \cdot \sqrt{\frac{2 \cdot n \cdot I}{\beta_D}}} \cdot \ln(C)$$

$$C = \left(\frac{1 - \frac{1}{\sqrt{1 + Gv}}}{1 + \frac{1}{\sqrt{1 + Gv}}} \right)$$

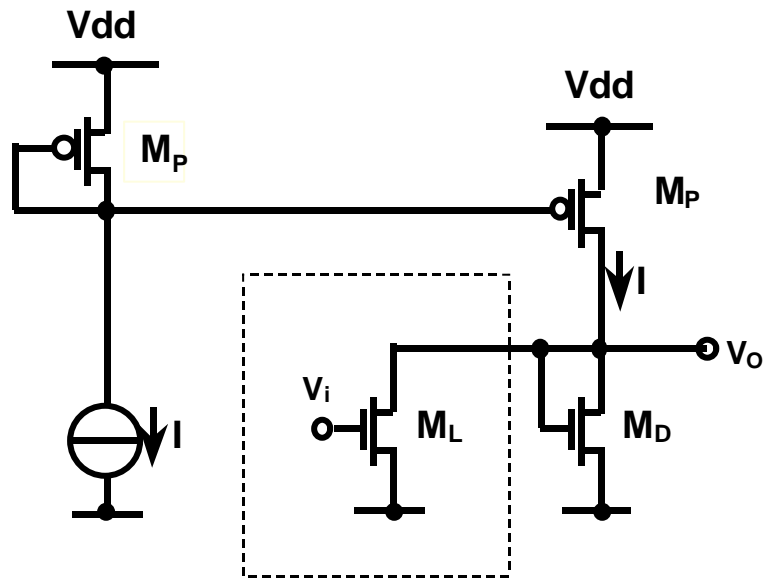
Region	M_L	M_D
I	ON - Triode	OFF
II	OFF	OFF
III	OFF	ON - Saturation
IV	OFF	ON - Saturation

Results - Propagation Time Validation

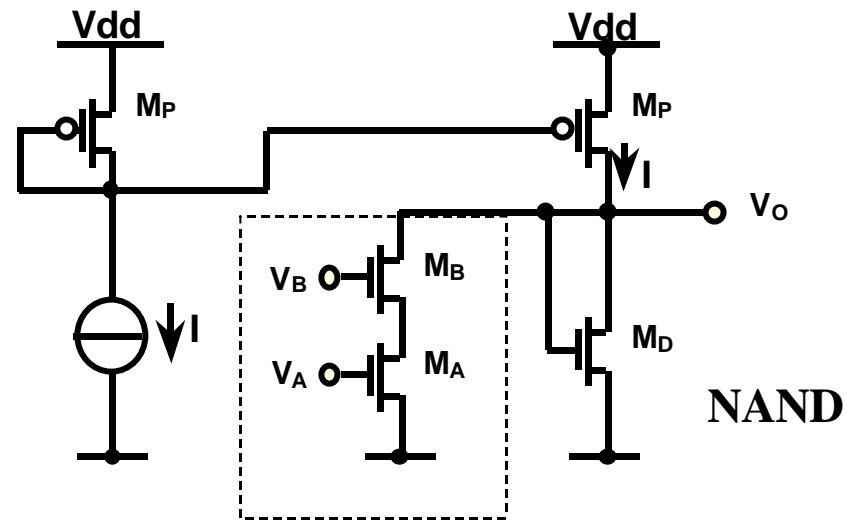


Results - CSL NAND and NOR Functions

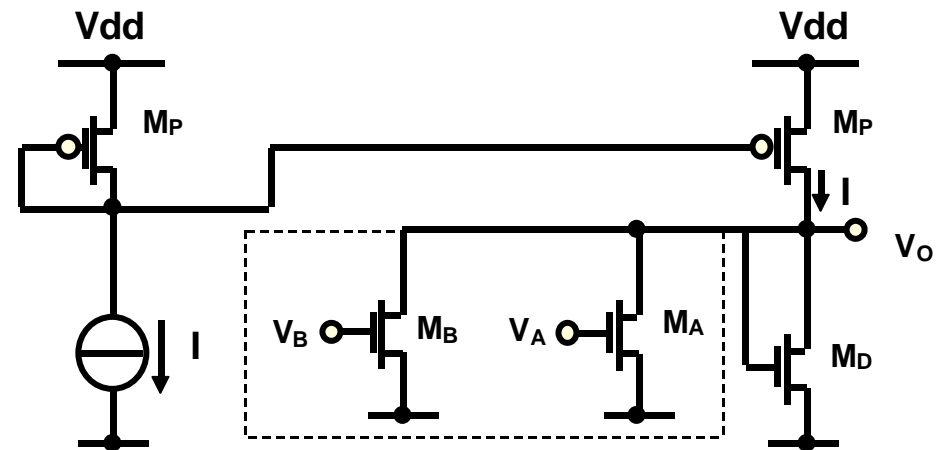
- ◆ More complex digital functions replacing M_L by associations of transistor (serie/parallel).



Inverter

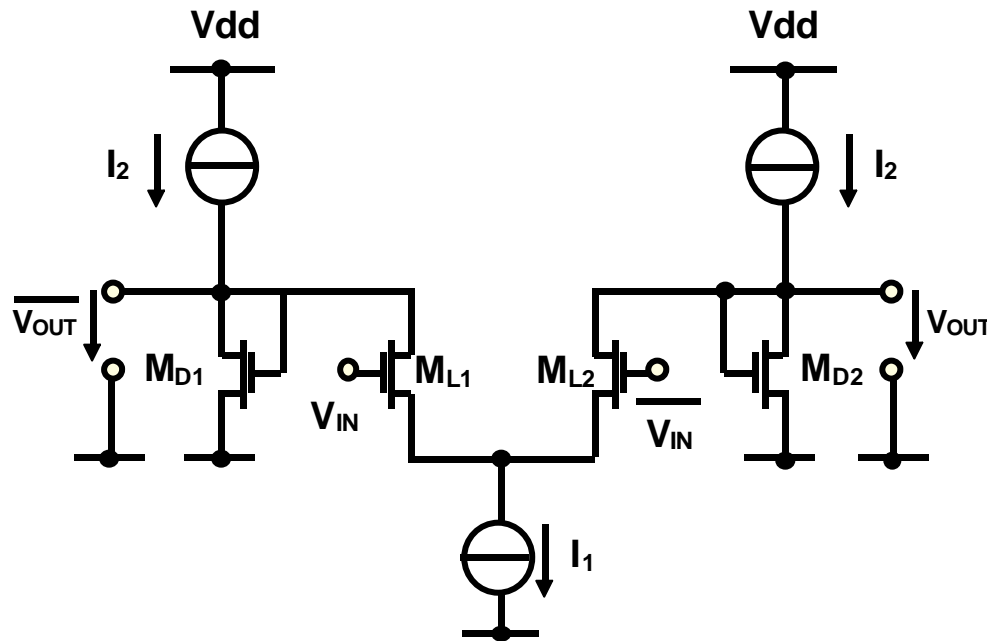


NAND

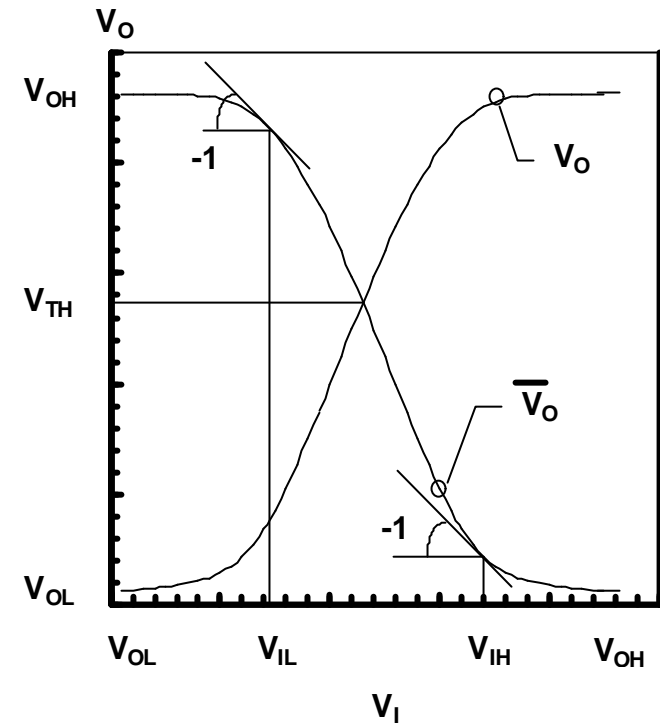


NOR

Results - FSCL Logic Family



FSCL inverter



◆ **x - parameter of design**

$$\xi = \frac{I_1}{I_2}$$

I_2 - constant
 I_1 - Variable

The higher the ξ the difficult are the matching constraints

Results - FSCL Inverter Static Characteristics

- ◆ Output high logic level

$$V_{OH} = V_{TON}^D + \frac{\Delta V_L}{1 - \sqrt{1 - \xi}}$$

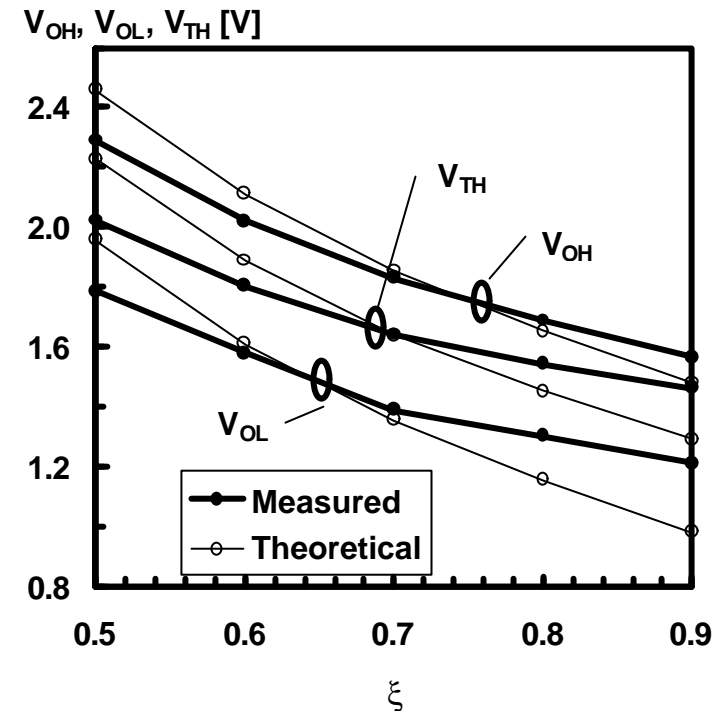
- ◆ Logic threshold voltage

$$V_{TH} = V_{TON}^D + \frac{\sqrt{1 - \frac{\xi}{2}}}{1 - \sqrt{1 - \xi}} \cdot \Delta V_L$$

- ◆ Output low logic level

$$V_{OL} = V_{TON}^D + \Delta V_L \cdot \frac{\sqrt{1 - \xi}}{1 - \sqrt{1 - \xi}}$$

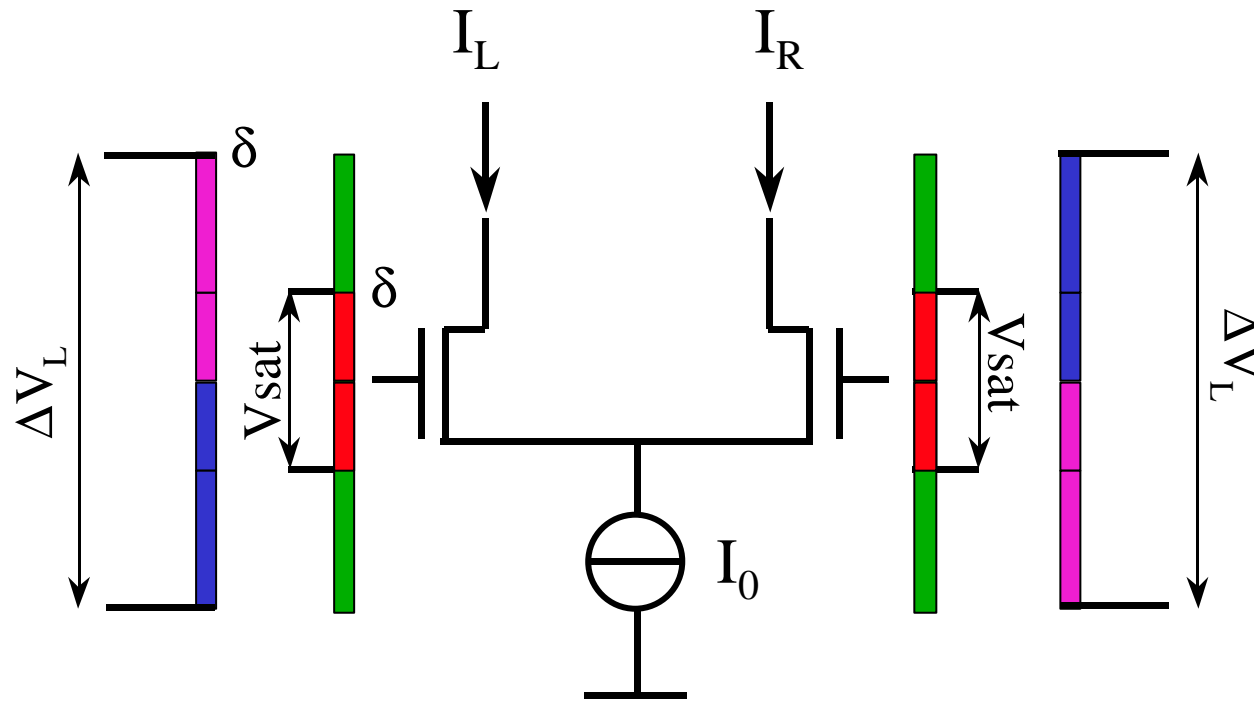
$$\Delta V_L = V_{OH} - V_{OL} = \sqrt{\frac{2 \cdot n \cdot I_2}{\beta_d}} \cdot (1 - \sqrt{1 - \xi})$$



- ◆ Constant noise margin and logic swing.

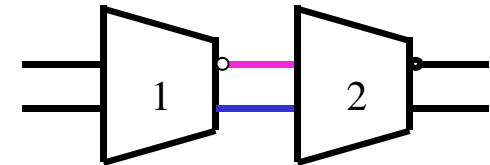
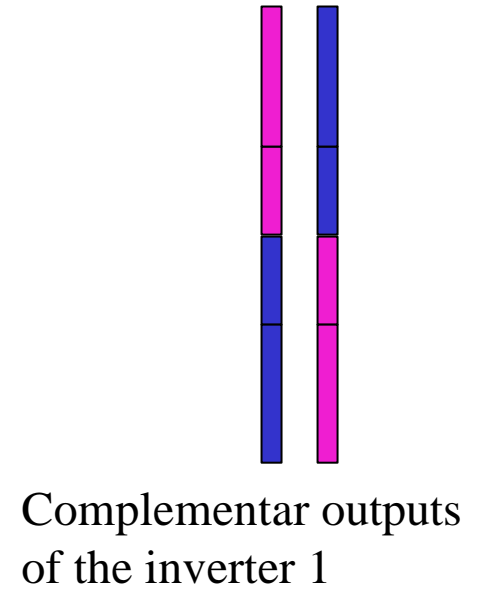
The larger the ξ the smaller can be the power supply voltage.

Results -FSCL Second Order Analysis



$$I_0 = I_L + I_R$$

Inverter 2



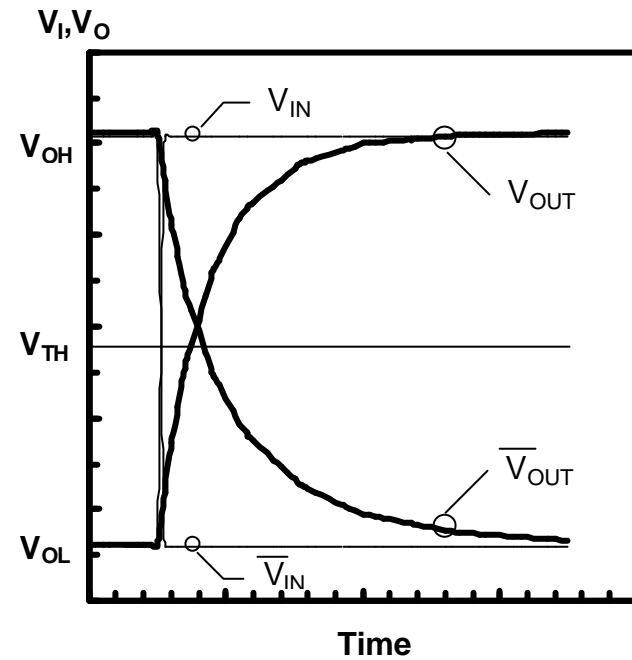
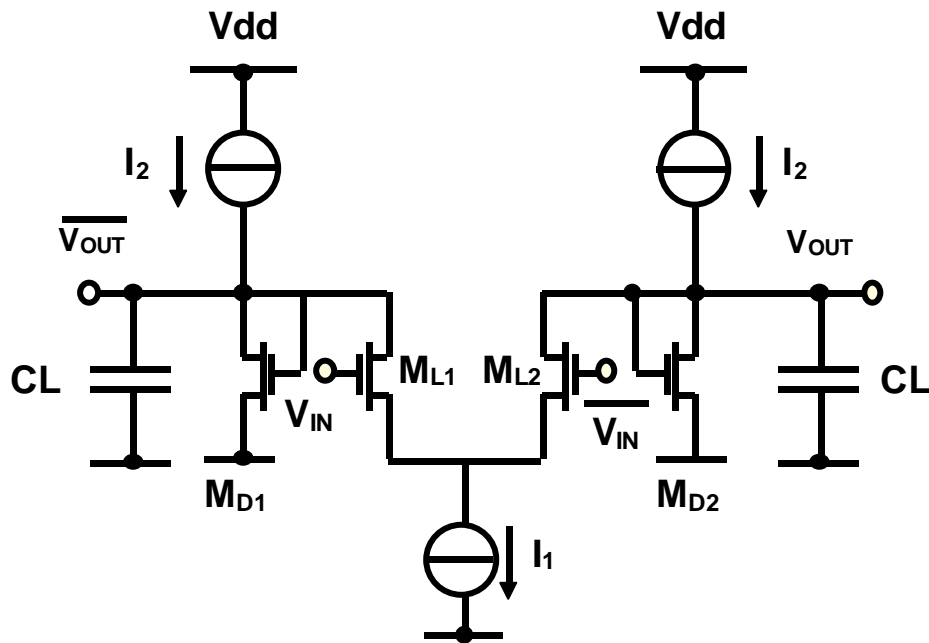
Results -FSCL Second Order Analysis

$$\begin{aligned}
 \sigma^2(\delta\Delta V_L) = & \left(\frac{1}{2} \cdot \frac{n \cdot g_{m_{RP}}}{\beta_{RP}} \cdot \sqrt{\frac{\beta_{RP}}{\beta_d}} \cdot (1 - \sqrt{1 - \xi}) \right)^2 \cdot \sigma^2\left(\frac{\delta\beta_{RP}}{\beta_{RP}}\right) + \\
 & \left(\frac{1}{2} \cdot \frac{n \cdot g_{m_{RP}}}{\beta_{RP}} \cdot \sqrt{\frac{\beta_{RP}}{\beta_d}} \cdot (1 - \sqrt{1 - \xi}) \right)^2 \cdot \sigma^2(\delta V_{TOP}) \cdot \left(\frac{g_{m_{RP}}}{I_{RP}}\right)^2 + \\
 & \left(\frac{1}{2} \cdot \frac{n \cdot g_{m_{RP}}}{\beta_{RP}} \cdot \sqrt{\frac{\beta_{RP}}{\beta_d}} \cdot (1 - \sqrt{1 - \xi}) \right)^2 \cdot \sigma^2\left(\frac{\delta\beta_d}{\beta_d}\right) + \\
 & \left(\frac{1}{2} \cdot \frac{n \cdot g_{m_{RP}}}{\beta_{RP}} \cdot \sqrt{\frac{\beta_{RP}}{\beta_d}} \cdot \frac{\xi}{\sqrt{\frac{1}{\xi} - 1}} \right)^2 \cdot \left(\sigma^2\left(\frac{\delta\beta_{RN}}{\beta_{RN}}\right) + \sigma^2(\delta V_{TON}) \cdot \left(\frac{g_{m_{RN}}}{I_{RN}}\right)^2 \right) + \\
 & \left(\frac{1}{2} \cdot \frac{n \cdot g_{m_{RP}}}{\beta_{RP}} \cdot \sqrt{\frac{\beta_{RP}}{\beta_d}} \cdot \frac{\xi}{\sqrt{\frac{1}{\xi} - 1}} \right)^2 \cdot \left(\sigma^2\left(\frac{\delta\beta_{RP}}{\beta_{RP}}\right) + \sigma^2(\delta V_{TOP}) \cdot \left(\frac{g_{m_{RP}}}{I_{RP}}\right)^2 \right)
 \end{aligned}$$

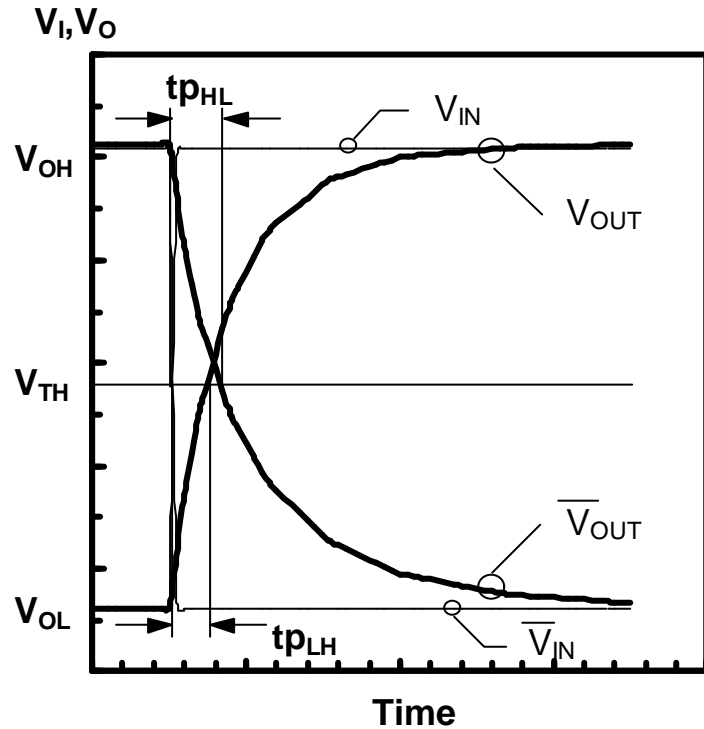
Results -FSCL Second Order Analysis

$$\begin{aligned}\sigma^2(\delta V_{\text{SAT}}) &= \left(\frac{1}{2} \cdot \sqrt{\frac{2 \cdot n \cdot I_{\text{RN}}}{\beta_{\text{L}}}} \right)^2 \cdot \sigma^2\left(\frac{\delta\beta_{\text{RN}}}{\beta_{\text{RN}}}\right) + \\ &\left(-\frac{1}{2} \cdot \sqrt{\frac{2 \cdot n \cdot I_{\text{RN}}}{\beta_{\text{L}}}} \cdot \frac{g_{\text{mRN}}}{I_{\text{RN}}} \right)^2 \cdot \sigma^2(\delta V_{\text{TON}}) + \\ &\left(-\frac{1}{2} \cdot \sqrt{\frac{2 \cdot n \cdot I_{\text{RN}}}{\beta_{\text{L}}}} \right)^2 \cdot \sigma^2\left(\frac{\delta\beta_{\text{L}}}{\beta_{\text{L}}}\right)\end{aligned}$$

Results - FSCL Inverter Dynamic Characteristics



Results - FSCL Inverter Propagation Times



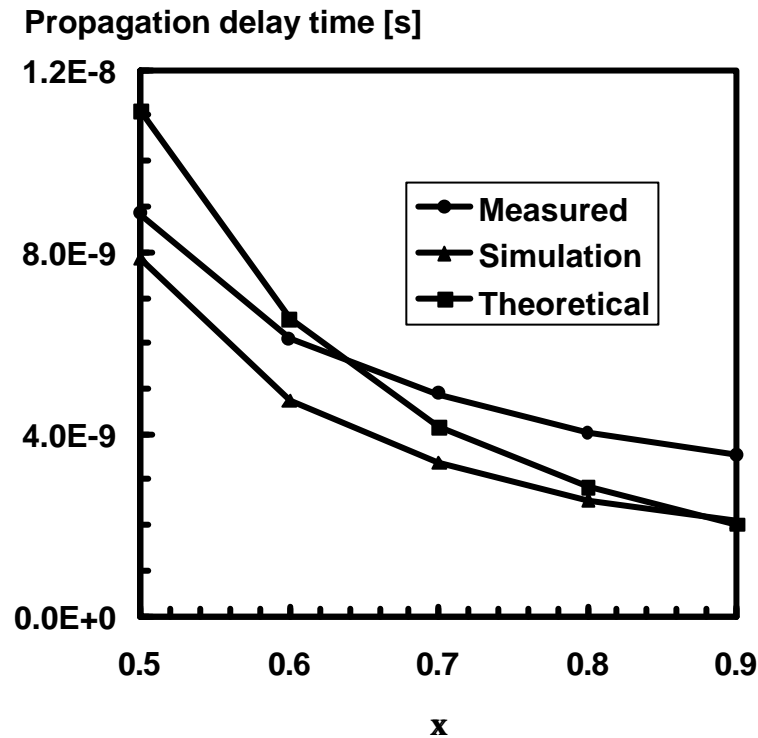
◆ Low to high propagation time

$$tp_{LH} = \frac{\Delta V_L}{2} \cdot \frac{1}{I_2} \cdot \frac{CL}{1 - \sqrt{1 - \xi}} \cdot \ln \left\{ \frac{\sqrt{1 - \xi} - 1}{\sqrt{1 - \xi} + 1} \cdot \frac{\sqrt{1 - \frac{\xi}{2}} + 1}{\sqrt{1 - \frac{\xi}{2}} - 1} \right\}$$

◆ High to low propagation time

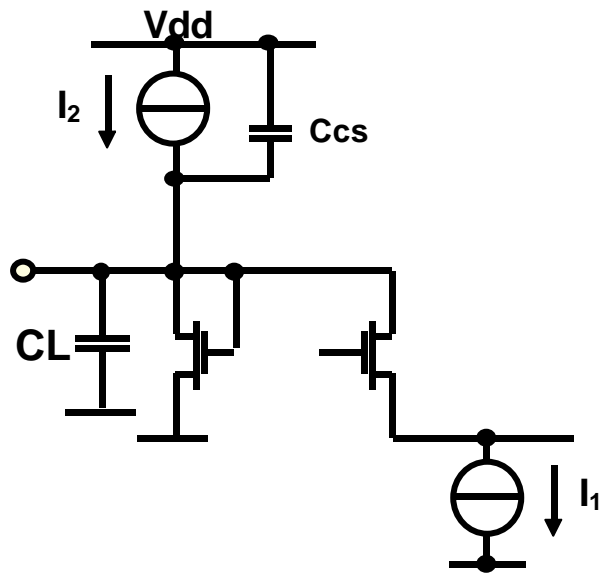
$$tp_{HL} = \frac{\Delta V_L}{2} \cdot \frac{1}{I_2} \cdot \frac{CL}{\sqrt{1 - \xi} - 1 + \xi} \cdot \ln \left\{ \frac{\sqrt{1 - \frac{\xi}{2}} + \sqrt{1 - \xi}}{\sqrt{1 - \frac{\xi}{2}} - \sqrt{1 - \xi}} \cdot \frac{1 - \sqrt{1 - \xi}}{1 + \sqrt{1 - \xi}} \right\}$$

Results - FSCL Inverter Propagation Delay Time



The higher is ξ the smaller is the propagation delay time

Results - FSCL Current Spike



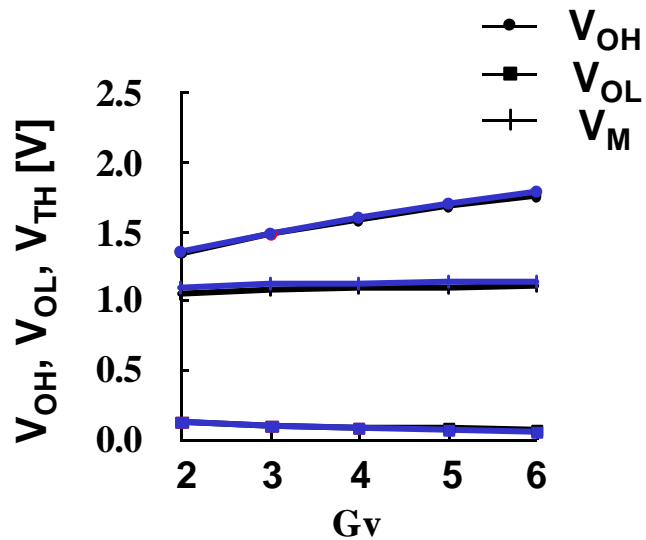
$$IN_R = -\frac{C_{CS}(\xi)}{C_L(\xi) + C_{CS}(\xi)} \cdot I_2 \cdot \xi$$

$$IN_F = +\frac{C_{CS}(\xi)}{C_L(\xi) + C_{CS}(\xi)} \cdot I_2 \cdot \xi$$

The resultant current spike is zero.

Results - Comparison CSL x FSCL

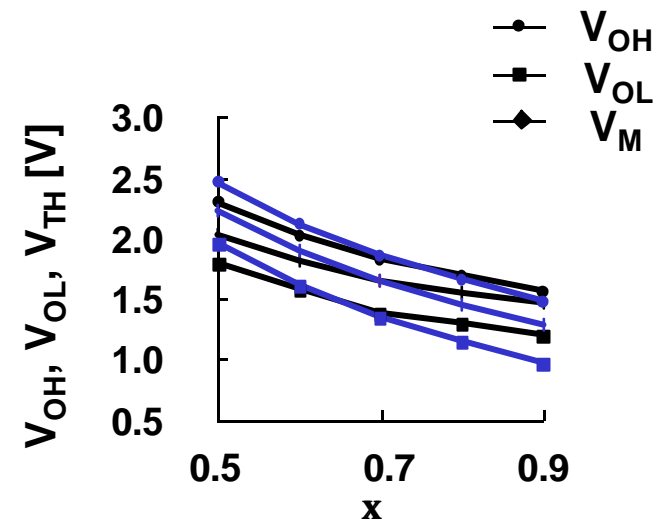
CSL



$I_1 - 20\mu A$

Calculated
Measured

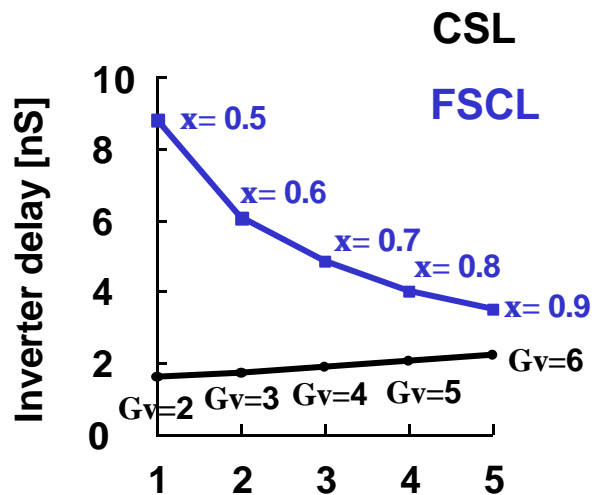
FSCL



$I_2 - 10\mu A$

Static Characteristics (same power consumption)

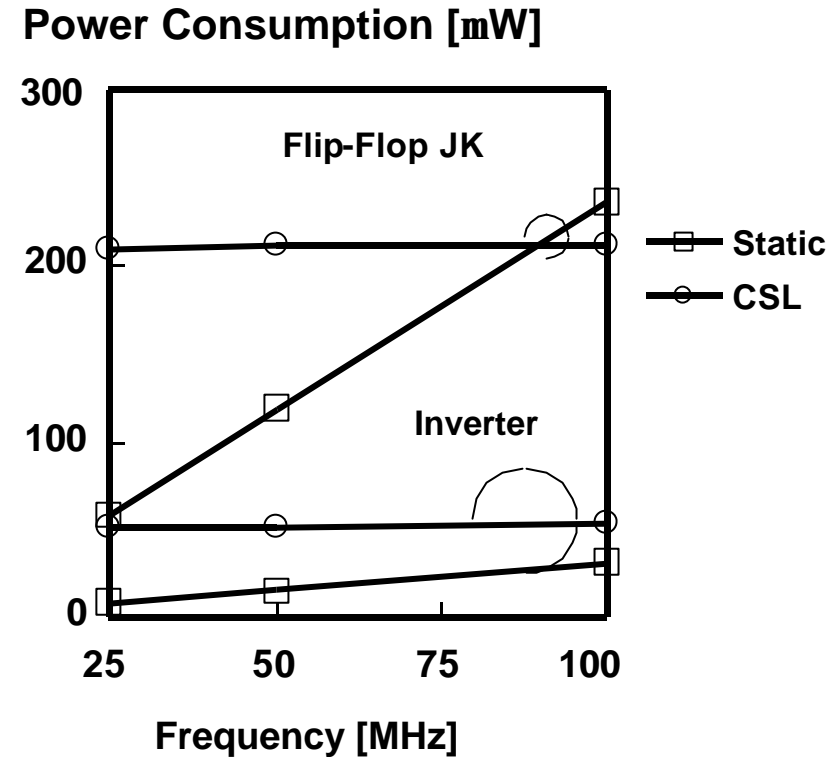
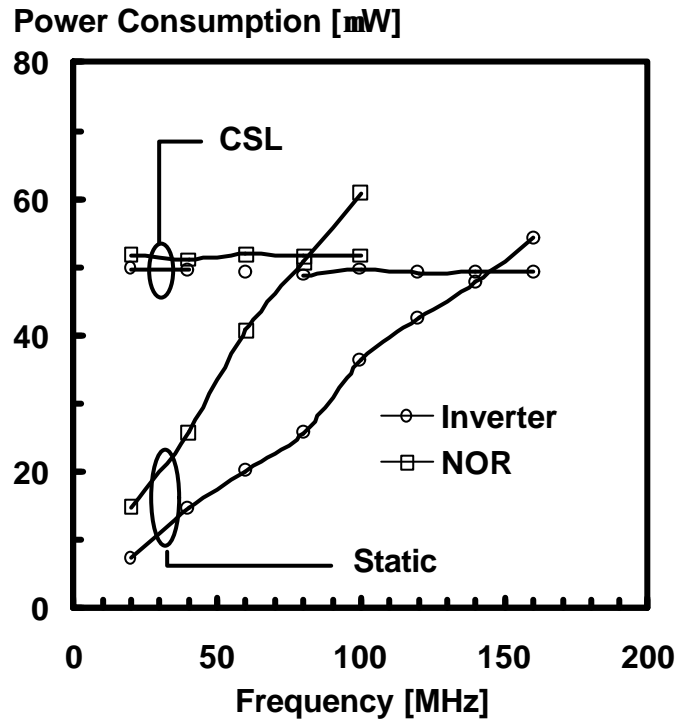
Results - Dynamic Comparison CSL x FSCL



Conditions :

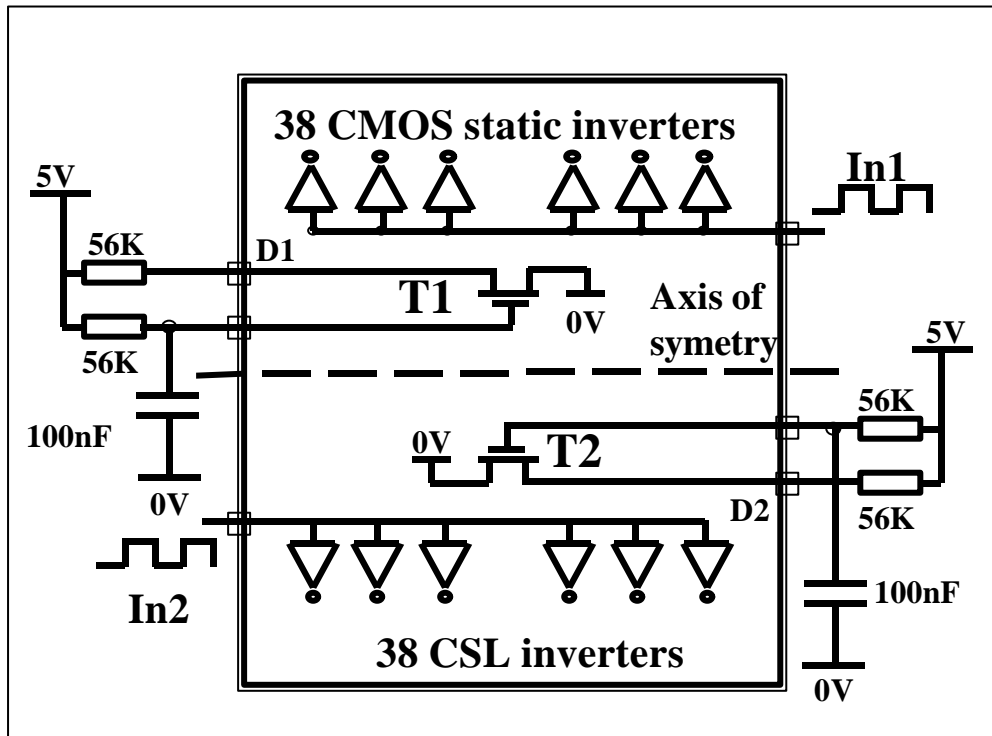
- ◆ Voltage Supply 2.5V
- ◆ Power Consumption : 50 μ W
- ◆ Same noise margins

Results - Power Consumption Comparison

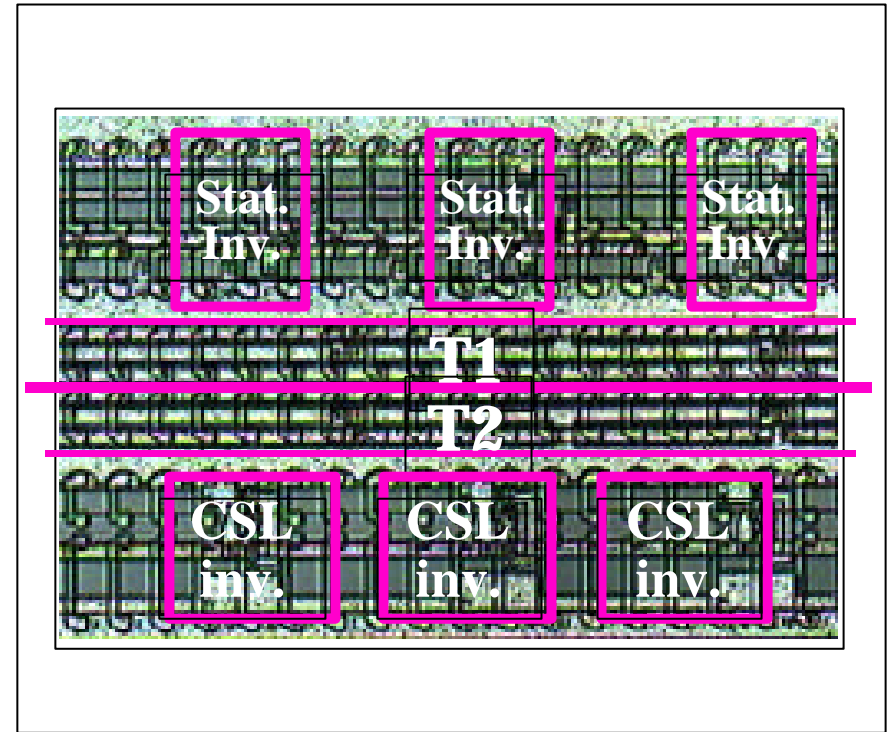


Under high switching activity condition, there exist a breakpoint where CSL consumes less power than the std static logic.

Results - Comparison of Noise Generation

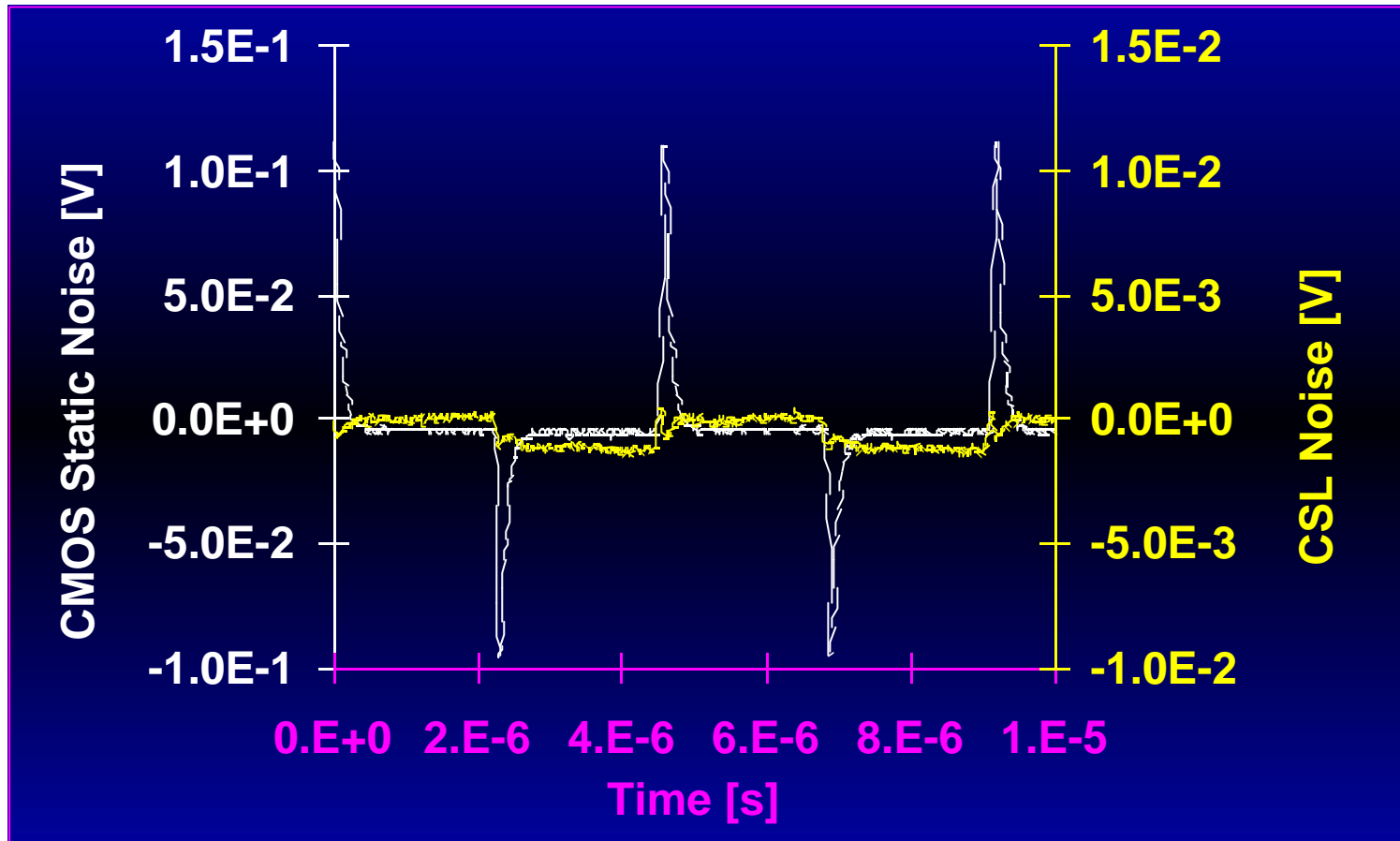


Schematic Diagram



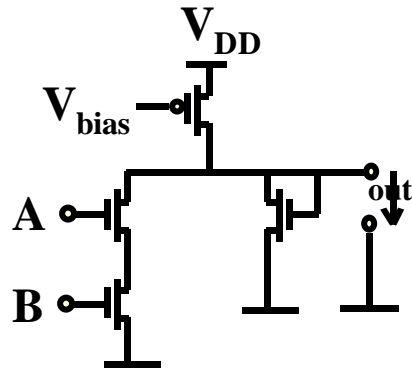
Chip

Results - Measurements of Switching Noise

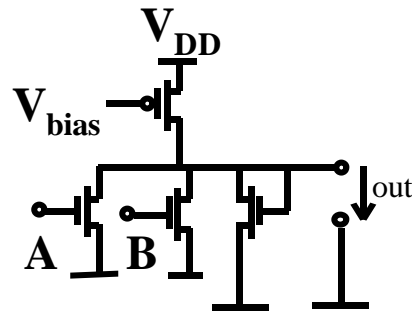


- ◆ $I_{\text{bias}} = 20 \text{ } \mu\text{A}$
- ◆ $V_{\text{DD}} = 2.5 \text{ V}$

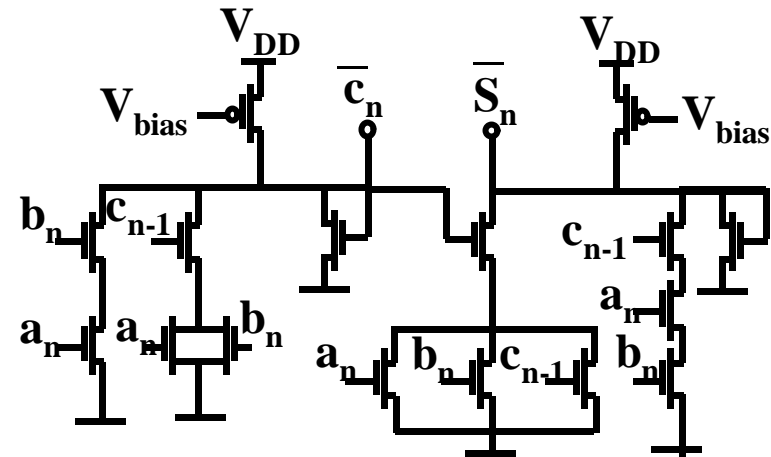
Results - CSL Cell Library



Nand



Nor



One bit full adder

- ◆ CSL library is ready for a top-down design flow.
- ◆ Layout of basic CMOS static gates is smaller than the CSL.
- ◆ When the number of inputs and the complexity of gates increase, CSL area becomes comparable.

Conclusions

- The reduction of switching noise in mixed-mode circuits can be obtained using current steering logic.
- The achieved procedure of design and the used design flow for the CSL logic demonstrate that this approach is ready for industrial applications.
- Power downing techniques and logic architectures with high switching activities are suitable for CSL power consumption.