

Panel on IP Demands for Mixed-Signal Testing

Validation Test Methodologies to Meet Mixed-Signal SoC Challenges

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The Importance of Mixed-Signal to Europe

- European lead in mixed-signal must be enhanced through efficient R&D activities.
- Current examples of European mixed-signal strongholds:

Biomedical

- Hearing Aids
- Health Care Monitoring
- Defibrillators

Automotive

- Stability Control
- Airbag
- Accelerometer Interfaces
- Collision Detection

Telecom

- Mobile Phones
- Optical Interface
- Set-top Boxes
- Phone/Cable Modems

Consumer Elec.

- Audio
- TV
- Multimedia(DVD)

The Challenge of Mixed-Signal IPs

- The analog and mixed-signal part of systems are typically providing the competitive advantages. So it is for mixed-signal IP-cell and SoCs.
- Problems associated with analog and mixed-signal typically lack structure and lend themselves much less to be handled by existing test & validation methodologies.
- Analog and mixed-signal will soon need to integrate RF and MEMS components – just increasing the level of complexity.

Mixed-Signal Test / Validation Dilemma

- Due to the nature and diversity of analog and mixed-signal, test methodologies are relatively poor automated for SoCs.
- The digital SoC approaches for test, including emerging structured approaches, have no similar existing alternatives for analog.
- BIST and DfT are almost non-existent in analog.
- Methodologies for handling analog and mixed-signal cores are often poor and need to be enhanced significantly.
- Linking between EDA tools and test tools is often weak.

Current Approach for MS IP-Core Validation

- The predominant approach is to use Extest (external mixed-signal test equipment).
- Extensive validation tests often manually generated but more and more based upon outputs for EDA environment.
- The linking between EDA and validation environment is essential to ensure optimal test generation.
- IP cells often have access for extra signals to ensure more efficient validation process.
- Validation test is performed by the originator of the cell, whether that is the silicon vendor or the system company.

Current Approach for MS IP-Core Validation

- Some major users that apply our IntegraTEST approach have an intimate cooperation with the IP vendor concerning the validation test.
 - Efficient results of cooperation in situations where the system house and the chip vendor can interchange information down to the validation test program itself.
- Results from the OPTIMSTIC project are successfully applied.

Future Needs/Trends

- Linking between design tools and test tools need improvements to facilitate an automated approach (e.g. a solution to export instrument setups in VHDL-AMS language to reproduce measurements on a “Virtual Tester”).
- Structured approaches must be researched and engineered, e.g. “IEEE1149.4/IEEE1500” like.
- Improved “Generic device” approaches to simplify validation testing.
- Methodologies for mixed-signal test assembly at block or system level.