

Model based Test Generation: A Means of Improving Test Quality and Time-to-Market in Mixed-Signal Test

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Abstract

In a quest for shorter time-to-market and higher test quality of complex mixed-signal IC's, a novel method for test generation and test program debugging, which can be applied prior to the availability of first silicon, has been devised. As a result, verification test can start when the first prototypes arrive from the foundry. The method builds upon using simulation engines combined with test software/ hardware as the basis for emulating complex chip functions. In this manner, electrically equivalent mixed-signal functions are created long before the actual chip functionality exists, and efficient test programs can be debugged on the basis of emulated complex mixed-signal functions. Since test program development and debugging can take place parallel to the manufacturing of chips, critical time gaps can be avoided, resulting in a significant shortening of development times for new mixed-signal chips.

The method is being applied in an industrial context for some of today's most chips for emerging applications in mobile telephony. The paper describes the major achievements and their effects as seen by leading manufacturer of mobile phones.

Keywords: Model based test generation, linking design and test, emulating DUT function, time-to-market

1.Introduction

Mixed-signal IC's, and particularly the analogue subcircuits of such IC's, have become the challenging bottleneck in testing of many of today's high growth application domains such as mobile phones, automotive, datacoms etc. Faced with a demand for shorter design and manufacturing cycles, higher quality and an ever-increasing complexity in chip size and functionality, existing methods for mixed-signal engineering test have proven insufficient and cumbersome for most design and test engineers.

A major difficulty often seems to be that due to the complexity of the functions on chip, it may take 1-2 months just to debug a mixed-signal test program, after first silicon prototypes have been received from a chip foundry. So even if a test program could be generated in advance, the design validation time is typically delayed another 1-2 months, i.e. the time it takes to debug the test program. In business sectors like mobile telephones, where the market window of opportunity is short and where product life cycles may be shorter than

one year, such unexpected delays are becoming prohibitive.

Over the last two decades many efforts have been employed to improve the general situation of time-to-market in the design and test domains. Not least in the field of complex chip design, the work has been several advances. The eightieth was the decade of solving test problems as an afterthought by involving massive test engineering to compensate for chip engineers lack of knowledge in how to handle the test and quality issues of a given chip function. The design process itself typically was handled in a sequential manner where hardware design basically had to be finalised before software design started, and eventually test engineering started.

In the industry, a general consensus existed since the beginning of the ninetieth that the existing approaches of isolated hardware software paths were less than optimal. To bridge this, new approaches like hardware-software co-design / co-verification- have started

to emerge in the second part of the ninetieth, e.g. a design environment like Mentor Graphics' *Seamless* [Ref. 1,2]. This has undoubtedly led to significant savings in the total design time. However, prototype validation and test in general of mixed-signal IC's are still basically left as an activity to be handled by test engineers as a rather isolated approach after the chip design is completed. Customers report that up to 25-35% of the time and cost for getting an integrated circuit to the market are test related, with test of design and debugging taking a substantial share of this.

The emerging first decade of the next millennium will see yet another set of new methodologies. Promising candidates are beginning to materialise. In the area of mixed-signal test, *Virtual Test* [Ref. 3-6] is one such candidate. Here the chip functions, the test systems to be applied for tests of such chips as well as the fixture interface between device and test system are modelled. Using these methods, the entire tester to device-under-test (DUT) performance can be simulated at a relatively simplified level and hence used for generation of an adequate, first approximation of a test program, including obtaining a certain element of automation in test generation as well. The advantage of this approach is that the generation of this first simplified test program, including the debugging of it, can be executed on workstation rather than an expensive test system with limited availability for design engineers. Due to the complexity of modelling, however, typically only less accurate and complicated test are suited for this type of generation.

The approach of *Model based test generation*, as presented in the present paper, is another

promising techniques that seems likely to be rather useful to many complex analogue and mixed-signal test problems. Particularly. if the aim is to obtain high quality in test and at the same time meet the time-to-market objectives and to offer a close coupling between mixed-signal design and test, the approach seems attractive just for the very reason that it provides a model and a technique for designers taking higher responsibility of the mixed-signal test. In contrast to Virtual Test, the Model based test generation test approach requires both a workstation and some active test hardware. However, the approach lends itself much better for generating more detailed and accurate analogue tests, often generated at the block level of function. As with virtual test, the test generation in Model based test generation can take place prior to receiving first silicon.

2.Objectives

The need for improved methods has grown out of the time-to-market requirement and a widespread cry in the mixed-signal community for better handling efficiency of complex mixed-signal IC's during test generation. Conventional methodologies for mixed-signal design and design-to-test do not support these requests well. Fig.1 presents the conventional methodology for mixed-signal design and test development.

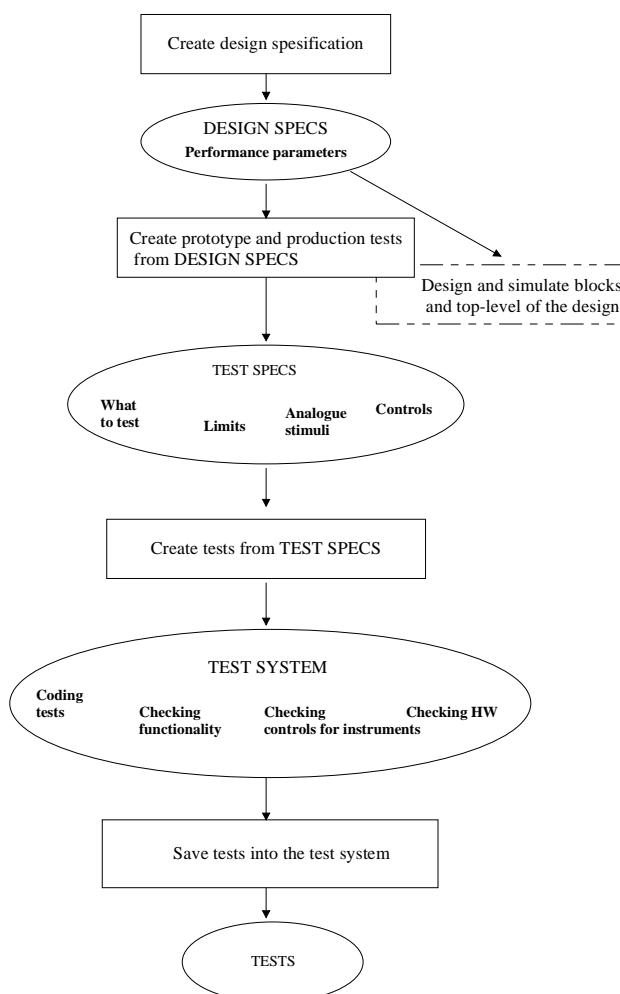
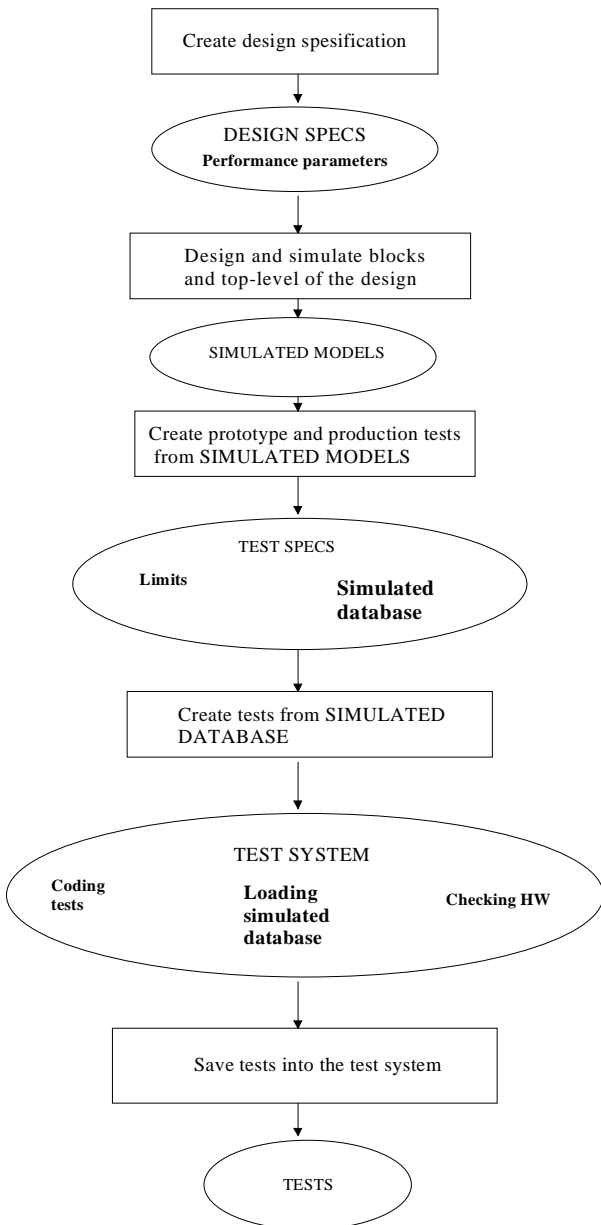


Fig.1. Conventional methodology of mixed-signal design and test development.

In consequence of this, the development of a new approach was decided. The active players in devising this approach, in the following referred to as *Model based test generation*, were chosen to represent in-depth knowledge of the problems from user point of view as well as from tool development point of view.

The basic objective of the Model based test generation approach was to generate and debug the test program for a mixed signal chip design before the hardware is built. This would allow reducing the overall validation and debugging time associated with new mixed-signal prototype chips and hence improve the time-to-market in the fast evolving business segment of mobile telephony. Another important aim was to reduce the entire job of creating a test and validation suite for new complex mixed-signal components. This means improving the program development productivity significantly and allow the user company to handle even more complex solutions within a reasonable resource.



It was planned to show clear improvement over existing design verification/validation techniques for mixed-signal applications. Reductions in the test cost (e.g. improved productivity, lower total costs, etc.) were clear objective. Part of the strategy was to obtain better technical performance in terms of accuracy and improved measurement techniques such as multi-tone testing and other DSP based testing methods. Improved transfer of results from the mixed-signal design environment was also seen as an important aim, and so was the ease-of-use and openness of the approach.

3.A principle of Model based test generation

Over time, software has become a major element in improving functionality and performance of test systems. A larger and larger part of the system owes its functionality to advanced system tools. This also applies to the approach taken in Model based test generation.

We chose the name Model based test generation, because the principle applied uses a simulation environment to emulate the given mixed-signal function. This emulated function is then used for driving electrical generators that generates the given electrical signals. Hence complicated equivalent electrical signals can be generated emulating the electrical signals that the designed chip will eventually have when first silicon is available. As a result an electrical signal suite is available for debugging of test programs long before actual silicon can be made available. Fig. 2 shows the method for Model based test generation.

The rationale for the Model based test generation is that in the verification approach used by the major user hitherto, the debugging of test program used for chip validation (verification) cannot start until the first prototype hardware is delivered from the chip foundry. Since debugging of the test program is now from typically 3-4 weeks up to 3 months, valuable time is lost in the design verification process.

Fig. 2. Methodology of Model based test generation.

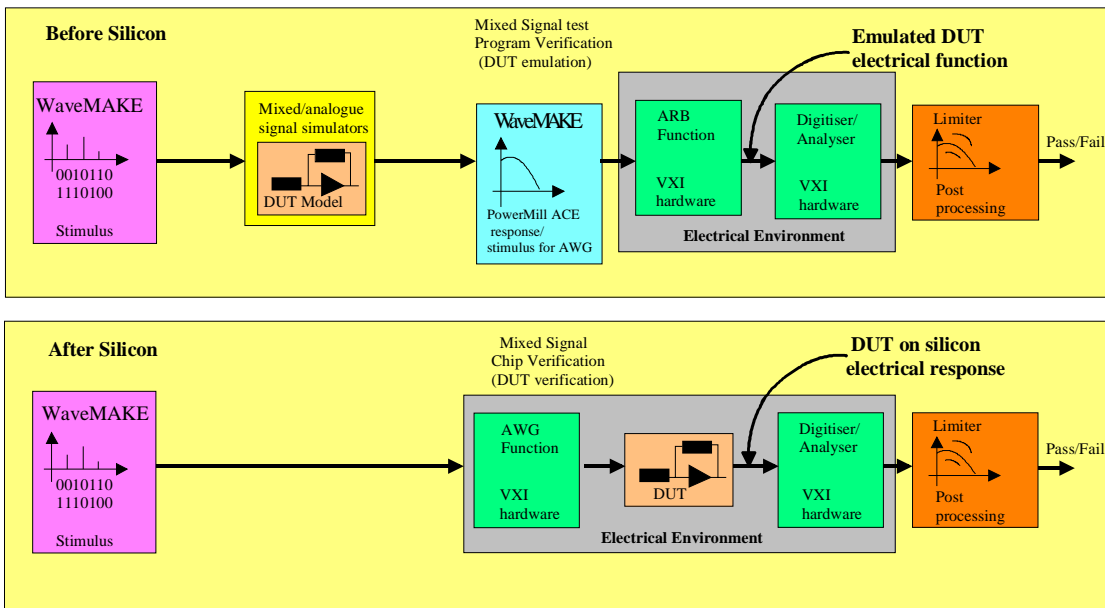


Fig.3: Illustration of a principle in Model based test generation. In the upper picture, the simulation of a given DUT function takes place. This stimulus is used for the electrical hardware to emulate the function. The function can then be used for test program debugging. In the lower picture, the actual chip is being tested using the hardware modules that were earlier used for test program verification.

The new approach, based on the Model based test generation principle, is to use the analogue and digital test hardware of the engineering test system as part of the emulation of more difficult electrical functions of the chip being prototyped, especially the analogue functions of this chip. This allows the verification of such functions to take place before the actual ASIC prototype is available. It further means that the test program itself can be verified before silicon is available.

The necessary function to drive the test hardware can be obtained from a mixed-signal simulator using the model for the given chip, or a subset of the functionality of this chip. Actually, it is likely to be the case in many situations that only a subset of the functionality is simulated in detail. The performance of mixed-signal simulators is restricting to reach maximum level of simulation complexity. Depending on the level of details required for the electrical function of especially analogue functions, the simulator may have to deliver some simulation at transistor level, while other functionality can be derived from higher level simulations. On the other hand the design can be portioned in simulation to different parts that the mixed-signal simulator handles on different levels. One level can be a transistor level, on e level can be a behavioural model level ,etc. The trade-off between simulation levels, provided that a hybrid approach is available, is an issue related to computational time accuracy of the electrical signal, ability to subdivide the chip function, etc.

The simulation task is no trivial task. To obtain the necessary accurate simulation result may take from several hours to days and in some case up to weeks, using a state of the art workstation (multi-processor architecture), even for a subset of the chip function and for may be only a few millisecond of actual test signals. Actually this is also a good indicator of difference between a mixed-signal test derived upon a Virtual Test approach and the Model based test generation approach. In virtual testing the modelling needs to be much simpler because the simulation needs to include the ATE system, the chip and the function. In Model based test generation may be only one D/A converter simulated, but simulation times are typically larger, because of the much finer level of granularity in the modelling. Detailed SPICE models may be required for much of the functionality.

Actually, at the outset of the reported development activity it was not the intention to necessarily cover entire chip functions. Rather, a devide-and-conquer approach was devised, since many mixed-signal chips have rather well defined functional elements that can be tested as isolated elements. Therefore it seems reasonable to emulate the same type of isolated functionality.

Another advantage for many applications of Model based test generation is the fact that typically only a few analogue pins exist in modern, complex mixed-signal applications, particularly DSP based mixed-signal chips. These "digitised analogue" signals lend themselves well for structured approaches like the one described here.

Having generated the necessary output responses for a DUT on the basis of simulation of this part of the chip, the stimuli and corresponding emulated responses can be transferred to an intermediate viewing and editing environment, a mixed-signal waveform editor. This tool, WaveMAKE [Ref. 7], allows the user to view and edit all the analogue, digital and digitised analogue signals for a given test. This tool offers links to mixed-signal design systems like Cadence and Mentor. The WaveMAKE tool also has embedded functions for converting between analogue and digital domains. For example, converters were developed for converting an analogue signal to a digital PDM format or vice-versa. It is also possible to run FFT analysis of analogue as well as digitised analogue signals, for example a PDM signal.

When the simulator response is transferred to the WaveMAKE waveform editor, it can be used as input to a given test hardware, e.g. an arbitrary waveform generator. At the output of the generator, the difficult function now appears and can be used for debugging the test and verification program concerning the given difficult analogue function. Hence, the time consuming part of debugging process may now take place in parallel to the prototype manufacture of the ASIC itself.

The emulation of the chip function is a main principle in this approach. Although it may be applied in general, it has not been the ambition to necessarily introduce a complete emulation of the chip. Even the emulation of a few major sub-functions may remove over 50 % of the time otherwise consumed for test program debugging after the first silicon has been obtained. If these functions are handled, using the emulation approach, this may prove to be the optimum solution. But it is always feasible to proceed to level where all functions are covered using the approach, although it may not prove fully cost effective.

After the emulation process, and following the supply of first silicon, the system is used for the full verification of the mixed-signal chip, using the coherent test capabilities of tester solution.

To yield an efficient approach, an integration of the engineering test (design validation tools) into the design trajectory was required. This link had to allow for fast mapping of design data into the engineering test environment, as well as mapping of experimental results from the hardware verification back to the design environment as well as mapping of experimental results from the hardware verification back to the design environment for new simulation undertakings. The latter is desirable in the case where the design verification has disclosed sensitivities or problems not originally detected during mixed-signal simulation. Re-simulation of the given circuitry with the new set of

boundary conditions can then determine whether the cause for non-detection in the first place was due to insufficient simulation requirements and conditions, or whether the problem was caused by use of inadequate models. As mentioned above, the WaveMAKE tool serves as a kernel for linking the design and test environments. Filter functions control the transfer of data from the design database into the database of the waveform editor. From here the data can be downloaded to the test hardware. Transfer of 1 Mbytes of generated test vectors typically takes 6-7 seconds.

In general, the interface tools have been optimised for high efficiency and throughput to reduce the idle time during test program development. During the development of Model-based test generation filters, called also bridges, has been developed for Accusim II and Continuum simulators from Mentor Graphics, PowerMILL ACE from Synopsys. In addition digital module SR2500 and digitizer TVS641 have got their own bridges.

4. Test system approach

The test system concerned is a series of test systems focused on a variety of application sectors but having a substantial part of the main software platform common for the systems of the different application domains. This prototype system meets the requirements of the user by offering the openness, modularity and not least the performance and it is planned integrated into applications of the user. The test system is a microLEX Systems IntegraTEST.

The system solution to be introduced yields a variety of test features like DSP based test techniques for A/D and D/A converters, a wide range of mixed-signal functions. Test features include for example: multi-tone testing, noise testing and a large number mixed-signal testing capabilities, all operating in a coherent mixed-signal test environment.

An important feature of the system is the integration of the mixed-signal simulation software with that of the verification system. Fig. 4 shows the basic idea of test system IntegraTEST. The basic aim is to manipulate different type of signals in a true, common mixed-signal environment. Whether preparing for mixed-signal test and verification or actually performing test of mixed-signal components, the issue remains difficult. In the mixed-signal environment we need a tool to be able to combine analogue waveforms and digital signals in a common visualisation window, and have access to support facilities for generating and manipulating signals, integrating signals generated through mixed-signal simulation, adding constraints, for example noise. On the other hand, the tool has to be able to combine results from several simulators to be for use in test. Simulation of complex mixed-signal

designs is often based on partial simulation results with inputs from analogue simulators like SPICE and digital ones like VHDL based or mixed-signal simulators like PowerMILL ACE. In this case design can be behavioural models or transistor-level models. During the development of this method transistor-level models were simulated in Accusim (SPICE) and PowerMILL ACE. Behavioural models have been simulated in Continuum (VHDL and HDLA models) and in

AdvanceMS (VHDL-AMS models). Modelling is described in detail in section 5. The tool must be able to allow signals from various sources to be assembled and organised with respect to each other, including phase relationships. Using a common window avoid problems of incorrect phases between analogue and digital signals.

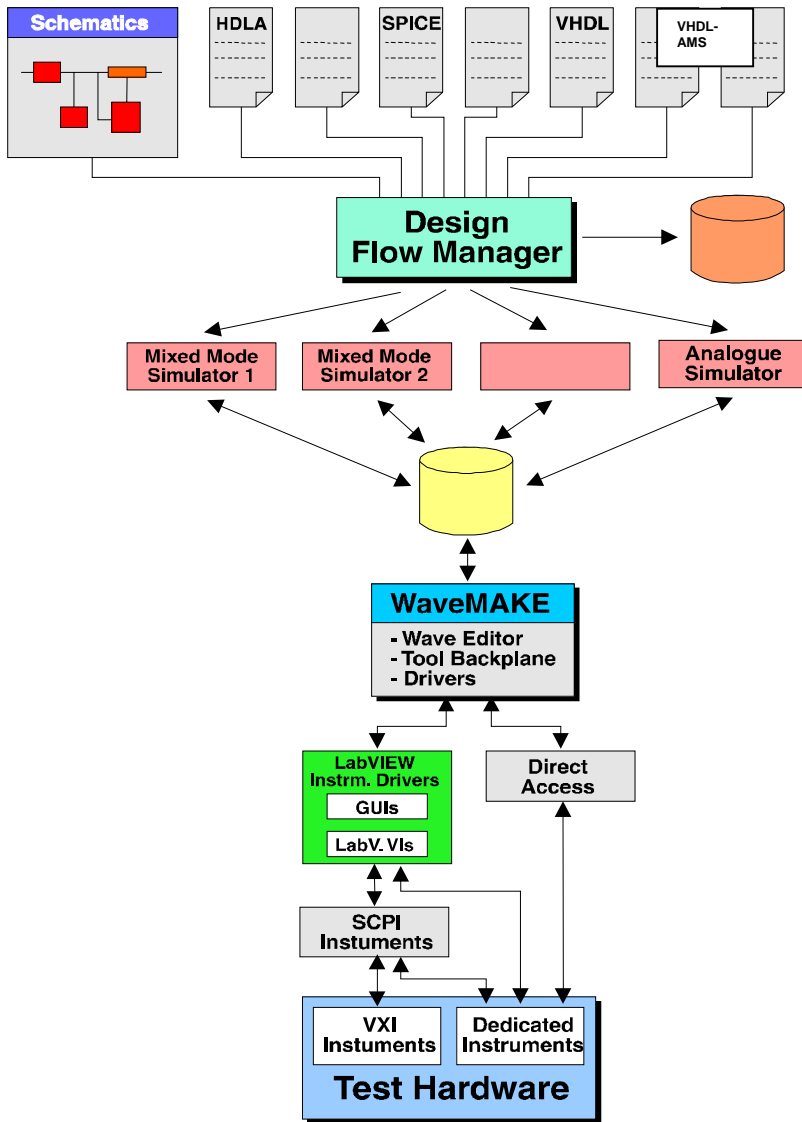


Fig.4. Interface between a design environment and the engineering test system

The system is planned to be applied for verification of prototypes, where the facilities offer quick programming and easy set-up as well as fast debug and hence faster time to market. The interface solution between mixed-signal simulation and mixed-signal test are an important part of solution. Such facilities will reduce the verification time even more.

It is of vital importance that the system performance be demonstrated in terms of:

- technical performance
- support for modern testing principles
- openness (inclusion of customers own developments)
- system throughput
- test quality
- total system cost

5. An implementation of Model based test generation

A. Test development and debugging

In traditional verification approaches, the debugging of the verification test program cannot start until the chip manufacturer has delivered the first silicon. Since debugging of the test program for the types of the chip in question is now typically from weeks to months, valuable time is lost in the design verification process.

The new approach, based on the experiment reported, is to use the analogue test hardware of the proposed test system to emulate the more difficult analogue functions of the chip being prototyped, and hence allow the verification of such functions to take place before the actual ASIC prototype is available.

To test the approach of Model based test generation an entire environment has been created that support the design to test interface as well as the hardware software tools for allowing an emulation of chip functionality, and hence test program generation and debugging prior to the delivery of first silicon. As test vehicle for the approach has been chosen a very advanced mixed-signal chip for mobile telephony application that the user company has conceived to date. The functionality of this chip consists of RF front end, a block for audio, filters as well as some additional functionality. The audio block presents quite some challenge in testing. The block contains converters based on modern design. This generates the need to handle PDM signal. The detailed functionality of the chip will not be presented here.

The measurements to be applied can be categorised as follows:

- DC measurements (currents, resistances, offsets)
- AC measurements (frequency response, distortion)
- Transient measurements (distortion, signal-path)
- Noise measurements
- Multi-tone testing

The test hardware in IntegraTEST is based upon a multi-vendor, VXI-based solution using open software environment. Instruments are from VXI bus instrument manufacturers like Hewlett-Packard, Tektronix, National Instruments, Interface Technology, and Bruel&Kjaer. In addition the system contains three GPIB bus controlled instruments.

The software environment of the test system is extremely flexible and allows easy interfacing to the design environment. The kernel of the test software is the tests, which perform measurements above. These tests are developed and run under test sequencer SequentTEST by microLEX Systems. The test development is presented in Fig. 5.

Test generation is based on utilising simulation of blocks and top-level design. The control signals for IntegraTEST generate automatically by reading simulation database and converting database signals suitable for test instruments. In the mixed-signal point of view controls signals are very important, because manually their timing is very difficult to insert.

B. Modelling for test generation

Modelling is based on design blocks and the top-level of the mixed-signal ASIC. Codec was selected for a demo case. Codec (Codec RX path presented in Fig. 6) includes a one-bit digital-to-analog converter, a one-bit analog-to-digital converter, analogue filtering and gain stages. A digital block controls these blocks. Codec models are transistor-level ones, which has been designed during the basic bottom-up design procedure. Parallel to these models behavioural models, based on HDL-A and VHDL-AMS, were designed. In this case the design is a top-down methodology. Digital block model uses VHDL coding in top-level behavioural simulation and transistor-level models in top-level transistor-level simulations.

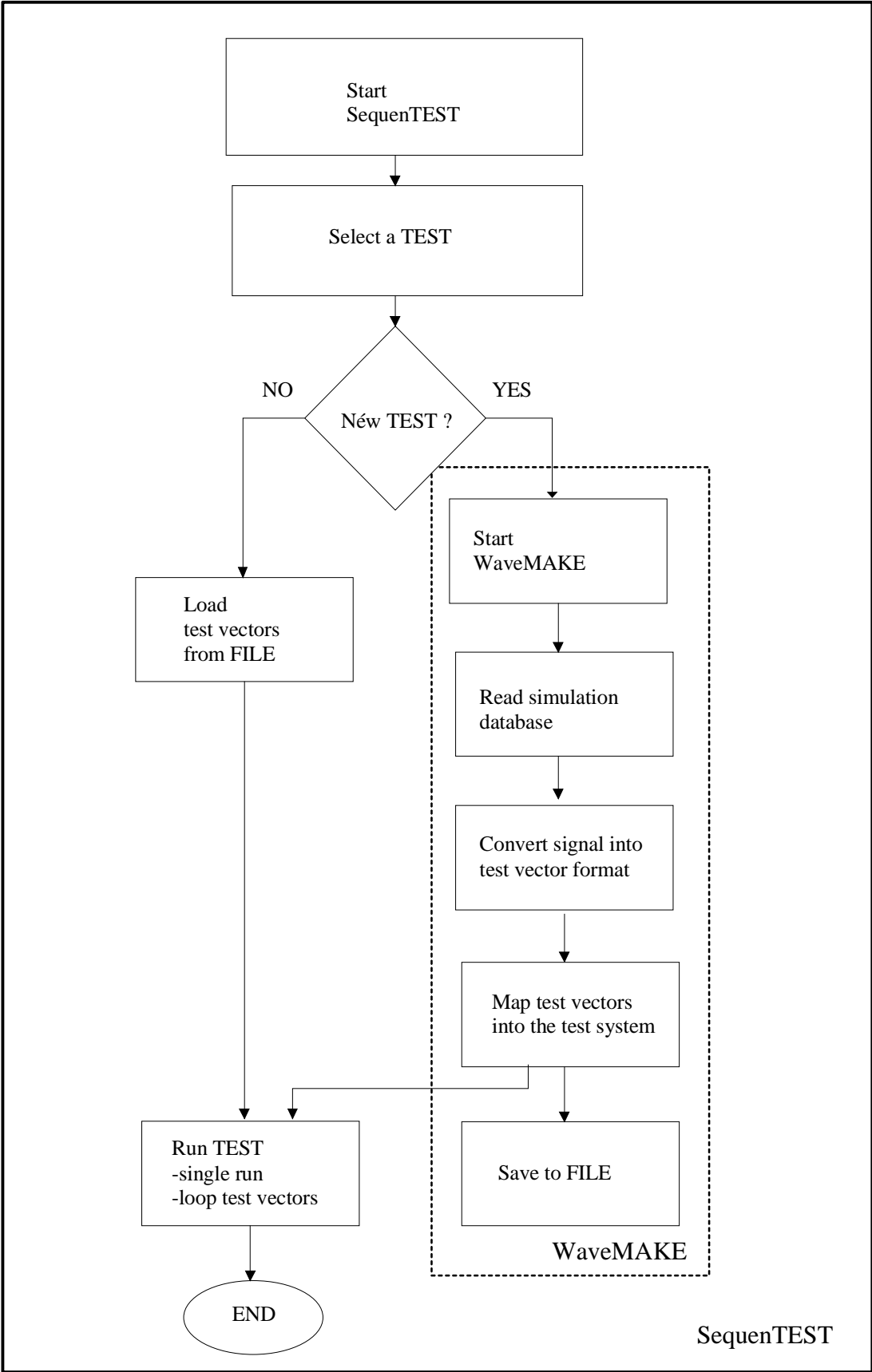


Fig.5. Test development and debugging in Model based test generation.

Table 3. Top-level simulation.

Block	PowerMILL ACE <i>Transistor-level Model</i>	Continuum <i>HDL-A – VHDL Model</i>	VHDL-AMS Design Station <i>VHDL-AMS Model</i>
TX path	48.5 hours	6.5 hours	Not done
RX path	31.0 hours	5.5 hours	Not done

Table 4. Mixed-signal test generation.

Function	PowerMILL ACE Transistor models	Continuum VHDL and HDL-A models
Startup <i>230 ms</i>	16 days	1.5 hours
Audio Codec TX path <i>15 ms</i>	48 hours	6.5 hours

As a result of this evaluation, the method allows the user to mix different models to create an accurate enough model for mixed-signal test generation.

All simulations have been run in Sun SPARCstation 450, which is driven by four CPUs at 450 MHz clock frequency with 4 GB cache memory.

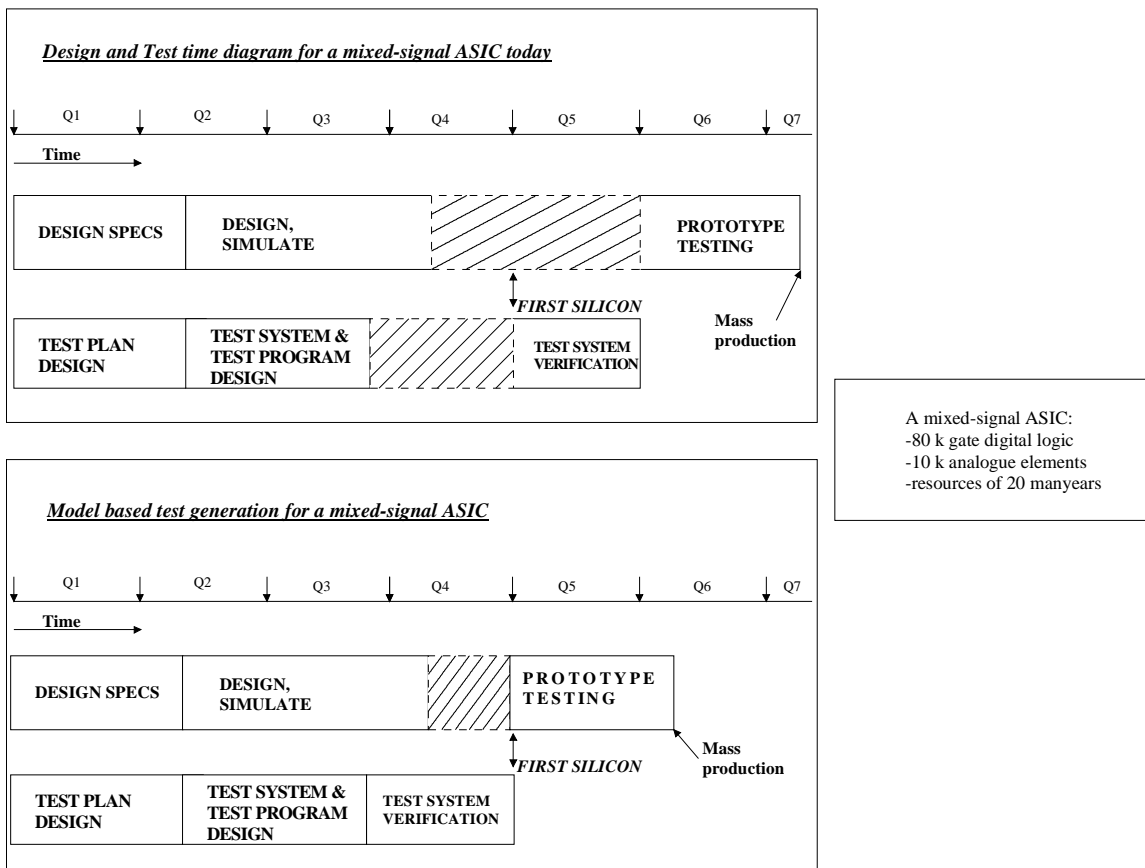


Fig 7. Time schedule for 1) traditional test development, 2) model based test generation

Table 5. Resource allocation of a mixed-signal design and test

Task	Design and test development TODAY		Model based test generation	
	Design Engineer	Test Engineer	Design Engineer	Test Engineer
Create design specification	X		X	
Simulate blocks and top-level	X		X	(X)
Create prototype and production test specification		X	X	
Create tests		X	X	X

6.Results

Results can be presented in three categories: influence on the design time schedule, influence on resource allocation for design and test and a demo test generation method.

The first result of studies with Model based test generation can be presented in a time schedule improvement. A typical time schedule for quite a complex mixed-signal ASIC is presented in Fig. 7 for both a traditional test development and a model-based test generation. The demo RX audio codec is one block of a complex mixed-signal ASIC.

In addition to time schedules resource allocation of a mixed-signal design and test is able to rearrange. The traditional two-sided design and test can emerge. A design engineer takes a more entire response of the block design and test. Test is part of real design process. Table 5 shows the resource rearrangement.

As a demo for Model based test generation a Codec RX path test generation methodology was implemented. In this case top-level simulations generate top-level models of Codec RX. These mixed-signals can be captured into WaveMAKE. In WaveMAKE the test engineer/design engineer set the vector formats for these signals and maps them into SR2500 digital module. Now the test has

the right controls and test stimuli. Fig. 8 shows the principle of the demo case.

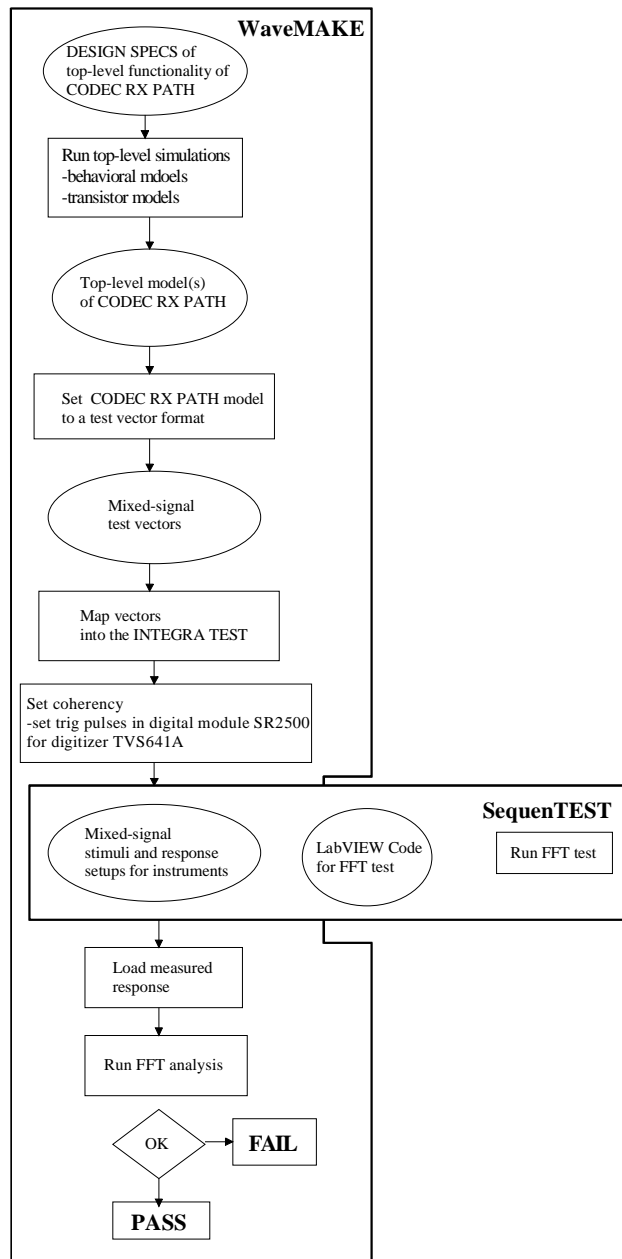


Fig.8. Codec RX path demo.

As a typical mixed-signal test the use of simulated signals as control and stimuli assumes to synchronise the analogue response and the digital stimuli. The synchronisation has not been provided in today's instruments as a self-clarity. In this case one pin of digital module SR2500 was used as a trigger signal. This signal was cabled to Tektronix digitizer TVS641A that captures the response of Codec RX path.

The test outputs the result into WaveMAKE which presents now the simulated response signals v_earn_,v_earp_,v_hf_ and v_hfcm_ and corresponding measured response signals m_EarN_,m_EarP_,m_HF_ and m_HFCM_ of Codec RX path. The evaluation figure is the FFT analysis of RX path output. Fig. 9 shows WaveMAKE display at the end of the test. The measured response and the simulated one can be compared and evaluated by FFT analysis.

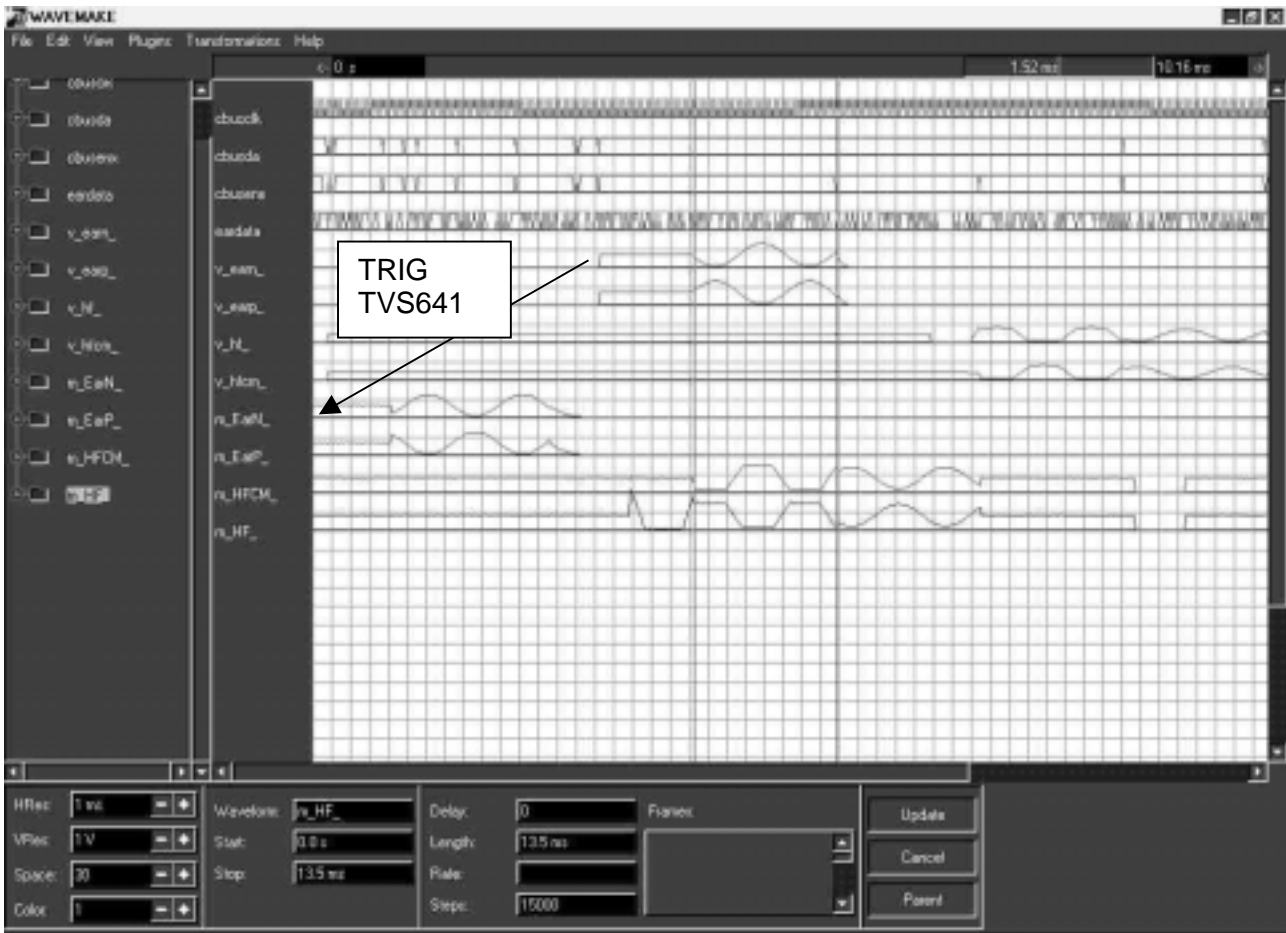


Fig.9. The demo test presented by WaveMAKE . Simulated and measured responses.

8.Conclusions

At this point in time, given the first successful experiments, it seems fair to conclude that the Model based test generation approach is a rather promising one for future applications in complex mixed-signal applications. Especially for digitised analog applications, where a limited number of input and output pins are present, the emulation approach taken appears the most optimal solution, given the complexity of the mixed-signal functions.

One direct result up to now has been to introduce new solutions in the ASIC design flow. The main result is

to demonstrate that the system approach is very applicable for verification of mixed-signal chips for the telecommunication area. The gains in total development time are extremely encouraging and indicate savings of weeks or even months in the total development time of such complex chips as undertaken in the present activity.

The general improvements in the flow can be measured in terms of:

- reduced time-to-market

- improved test performance/fidelity
- easy transfer of results from design to design verification, and possibly to production
- user-friendly and fast test programming
- the quality of the test itself
- improved test throughput
- homogeneous test/verification environment yielding improved correlation
- system openness and flexibility
- enhancements in test and test result documentation

9.Acknowledgements

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10.References

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