

Behavioral Test Generation Modeling Approach for Mixed-signal IC Verification

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Abstract

An application of behavioral modeling for mixed-signal test generation and applied results are presented. It is shown that test debugging can be provided in the verification test system before silicon by utilizing simulated behavioral mixed-signal models. Due to the behavioral modeling technique, the computational performance was enhanced to a level allowing efficient test development and debugging. Influence on efficiency in design methods is reported.

1. Introduction

Major technical improvements have made it possible to reduce design cycle time in the IC design. But quite little development work has been made in making the IC test-development cycle more efficient concerning mixed-signal design. Developing IC test programs for ATE is a time-consuming task that takes place near the end of design cycle. In mixed-signal test development test engineers haven't been able to automatically translate design simulation data into test patterns and stimuli tailored for the target test system. There has been lack of top-level mixed-signal simulation data and transfer mechanism into the test system. As a result, manual mixed-signal test vector generation followed by time-consuming test debugging causes a big delay in mixed-signal IC verification [1,2,3,4].

In this paper, a novel approach, utilizing top-level behavioral mixed-signal simulation followed by automated transfer into the test system, is presented. This method replaces manual mixed-signal test vector generation, generates the right mixed-signal stimuli (test patterns) in the target test system. Now, test engineers can fully debug their mixed-signal tests before first silicon in the test system, which is used in characterization or product verification.

2. Generic Test Generation Modeling

Behavioral modeling and simulators are mature to enable the designer to generate a set of mixed-signal test vectors. The set can be specified in the simulation phase as one simulation case and comprehensively in testing phase as one testcase. Generic test generation modeling generates mixed-signal test vectors by utilizing the behavioral model simulation database, from which the method generates tester instrument format test vectors. The method can be compared to the corresponding digital test vector generation.

In this method, efficient top-level simulation requires the use of a mixed mode (analog and digital) simulator. In order to achieve considerable simulation times, behavioral models of key analog and digital blocks were developed. So in this project, ADVanceMS, a Modelsim like mixed-

signal simulation environment was used. ADVanceMS supports several different description formats such as VHDL (behavioral and structural), VHDL-AMS (behavioral and structural), Verilog, SPICE/ELDO and C language.

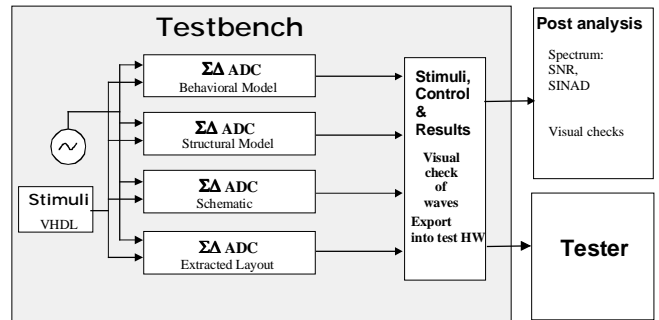


Fig. 1. The principle of generic test generation model.

In order to accomplish generic test generation, analog blocks are modeled by VHDL-AMS and digital blocks modeled by VHDL. These models are available in the early design phase. As the design process goes on, the SPICE/ELDO models are available, too. ADVanceMS accepts a multi-modeling hierarchy.

The principle of generic test generation model is shown in fig. 1. At the beginning a behavioral model of a sigma-delta converter is created. It specifies the converter. The structural model is meant to be used after the behavioral simulations to find specifications for the circuit blocks and to verify the operation with the most important non-idealities. The behavioral model describes the high level behavior of the system, and the structural model describes and models one possible implementation of the system in more detail. The simulation results of the structural model should be compared with the results of the behavioral simulations, as shown in fig. 1, to verify the correctness of the model development.

After simulations the RTL level VHDL description of digital part can be used in the logic synthesis, though the code may require some modifications. The correctness of the operation of the structural model should be verified by simulating it in the same testbench with the behavioral model and by comparing the results. The structural model can be used as a reference in later circuit simulations.

The main features and advantages of the structural model are two-sided. Specifications for the circuit blocks such as amplifiers can be determined and optimized. Behavior of the system can be simulated taking into account implementation specific non-idealities. The structural code can be used as stand-alone with ADVanceMS simulator, or it can be imported to design frameworks and used as a part of a larger system.

After high-level simulations with VHDL-AMS descriptions and finding block specifications these blocks can be substituted one by one with transistor level descriptions (schematics). This way larger systems can be gradually and more easily developed to full transistor level designs.

The simulation case, concretely the mandatory testbench, can be described in two ways. It can be a simulation sheet or a VHDL-AMS code. The simulation sheet is formed from the top-level design sheet by adding necessary analog generators for stimuli, response line terminations and a test vector VHDL model, which generates the digital control and is labeled by a generic test number. The designer selects the test number in the simulation phase. The test number links the simulation to the corresponding test case. For ADVanceMS simulation environment the simulation case is a SPICE netlist, which is shown in fig.2 and which includes VHDL models for both the digital block and digital test vector model (one block in the sheet) and VHDL-AMS models for analog blocks. The description of the test vector model is shown in fig. 4.

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Analog stimulus (current or voltage source):
V_I$189 miclp vss SIN( 1.35 0.5 3000 )

Mixed-signal test vectors (digital test pattern):
.MODEL TestHarness_ams(Harness_ams) MACRO
LANG=vhdlams LIB=work
Y_I$1240 TestHarness_ams(Harness_ams)
+ port : cbusclk cbusda cbusenx

Analog response (impedances):
C_I$9 vss earn 100p
C_I$8 vss earp 100p
R_I$6 earp earn 33

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Fig. 2. A netlist view of a simulation sheet.

The VHDL-AMS coded testbench, shown in fig. 3, describes the analog stimulus and simulated response as VHDL-AMS equations. The test case is, as earlier port-mapped test vector VHDL model in the testbench code. Similarly all simulated blocks, the digital block and analog blocks, are port-mapped into the testbench.

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--Analog stimulus:
v_miclp ==
0.5*sin(2.0*math_pi*3.0e3*NOW)+1.35;

--Mixed-signal test vectors (digital test pattern):
gen1: ENTITY TestHarness_ams(structural)
      PORT MAP(cbusclk cbusda cbusenx);

--Analog response (impedances):
v_earp== i_earp*R_LOAD;

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Fig.3. A VHDL-AMS coded testbench.

During and after the design phases of a mixed-signal IC it is important to verify the correctness of the developed models and descriptions, i.e. those descriptions at various phases have the same functionality and performance. For generic test generation it is important that the various descriptions (behavioral model, structural, schematic level, extracted layout) can be simulated in the same testbench using the same stimuli and test vectors (mixed-signal stimuli). The evolution of design is transferable into test debugging in real time.

3.Extracted Behavioral Test Generation Modeling

The test vectors, test stimuli and expected test response for test debugging are extracted from the design phase simulations, and the resulting signal formats are used for test vectors, test instrument setups of the analog generators and meters, measured responses.

Test vectors are set into tester acceptable format and mapped into the target pins of the digital module of the test system. The digital module generates mixed-signal test vectors in tests. The Mentor wdb-format database is handled by SimView list window. Selected time-equidistant signal are stored into a file, which the wave viewer WaveMAKE is able to import. WaveMAKE exports the database by utilizing its filters into the digital module in the test system. The digital module emulates the digital control of the mixed-signal chip. Extracting a behavioral testbench model, which is test case number 2 in the VHDL-AMS simulation, forms the digital control. In fig. 5 is shown the extraction of the digital control.

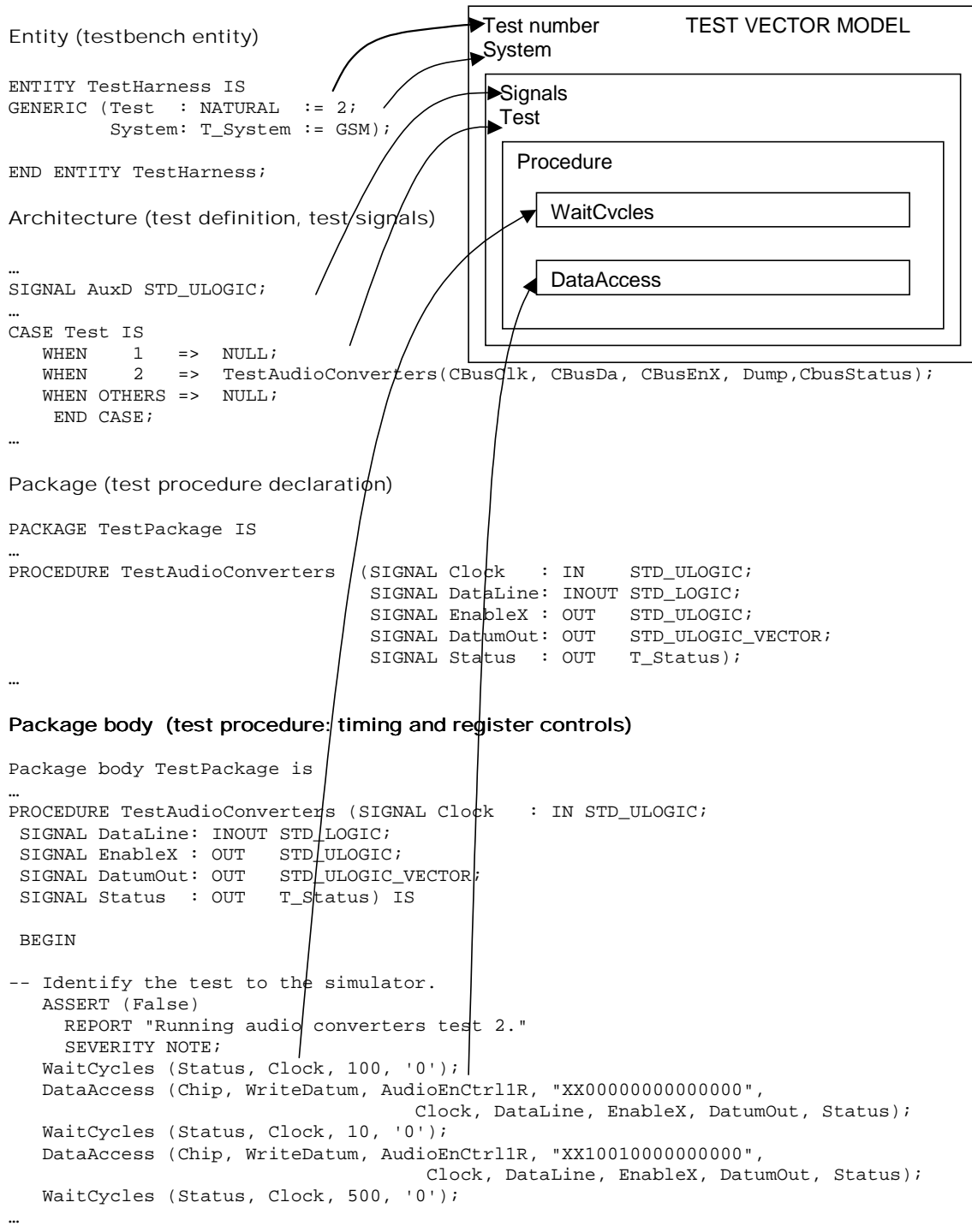


Fig.4. A test vector model.

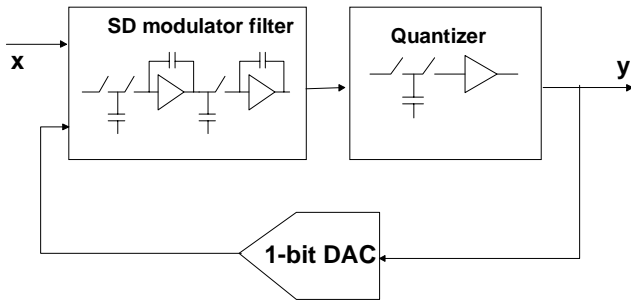


Fig. 8. A structural model of a one-bit second-order sigma-delta modulator.

Using specific filters tested extraction from simulation into the IntegraTEST. The filters format simulation data into tester specific format. Digital test vectors and digital stimuli/response of codec were mapped into SR2500 digital module, which is the physical description of the VHDL test vector model. The codec analog response signals were mapped into digitizer TVS641A, which respectively is the physical description of analog response. For evaluation of analogue transfer, it was used a DAC function of the codec. This method was presented in IMSTW01 [11].

5.Results

The generic behavioral test generation modeling means that verification tests are generated from simulated models. As a result we receive test specifications, which consist of extracted test generation models and test limits. Running an existing test is just a load operation and a test run. Running a new test consists of test coding, loading extracted database, test system HW checking and saving the test.

The testbench, used in modeling, is based on the top-level description of the device. The schematic based testbench is

a natural and automatic output of design process. It is conveniently a SPICE netlist, which is made by a netlister. Before netlisting it just exists a need to add stimulus and response elements, which further are the direct link to the instruments of the test system. Generic behavioral test generation can start immediately after the behavioral model of a sub-block is ready. A VHDL-AMS testbench has to be created manually, which supports to use the schematic based testbench as early as possible.

Mixed-signal behavioral modeling has been launched quite effectively during last years [7]. VHDL-AMS models are accurate; as well they are available early in a design process. The simulation times of top-level mixed-signal devices are now reasonable [8,9]. Related to conventional high-level descriptions, behavioral models describe the silicon and real signal values in interfaces.

Today reuse of design is very important in IC design and verification. This methodology supports reuse of verification as follows. Testcases emulate top-level simulations. Tests themselves can be transferred into different test systems. The extraction filter library defines the supported hardware. Test generation modeling is transportable into different design environments.

This approach helps test engineers' test vector setup, test debug and verification. Test engineers can perform IC test development prior to first silicon. Test development time shortens, the overall product development time as well, test development and debugging can occur in parallel with design, layout and fabrication. Savings in man-years can be seen in table II. In the research case total savings are 2.3 man-year resourcing. One big benefit is that simulation and verification cases can be merged. A second benefit is that this methodology creates accurate mixed-signal test vectors. The complex patterns have been verified in simulation. The signal coherency, which is necessary in mixed-signal test, is reached [10].

Table I. Simulation times for block level and top-level codec and block level performance (S/N [dB]) of the codec.

	Accusim	PowerMILL ACE	AdvanceMS Behavioral	AdvanceMS Structural
Block level	28 days – 79.52 dB	26.4 h – 51.5 dB	11 min – 86.5 dB	1.1 h – 81.5 dB
Top-level	NA	48 h	5.3 h	16.0 h

Table II. Resource saving in mixed-signal IC design and verification of the research.

Task	Design Engineer	Test Engineer
	Now / Savings [my=man-year]	Now / Savings [my=man-year]
Design Specifications	6 my / - 1 my	0 my / 0 my
Test Plan Design	0 my / +0.5 my	1 my / -0.5 my
Design & Simulate	8 my / 0 my	0 my / 0 my
Test System&Test Program Design	0 my / +0.5 my	2 my / -1 my
Test system verification	0 my / +0.2 my	1 my / 0 my
Prototype Testing	0 my / 0 my	1-2 my / 0 my
Design development gap	1 my / -1 my	
Test development gap		1 my / -1 my
ALL TOGETHER	15 my / -0.8 my	5-6 my / -1,5 my

6. Conclusions

Generic behavioral test generation modeling was shown to be technically suitable for generating and handling the complexity of mixed-signal device verification. Configuring mixed-signal instruments into a large amount of different testcases can be made in considerable time. New testcases, manually impossible, are feasible to take account.

One direct result up to now has been to introduce new solutions in the IC design-to-test flow. The main result is to demonstrate that the system approach is very applicable for verification of mixed-signal chips. The gains in total development time are extremely encouraging and indicate savings of months in the total development time of such complex chips undertaken in the present activity.

7. References

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