



## SUBSAFE

# Simulation Results of Basic Structures

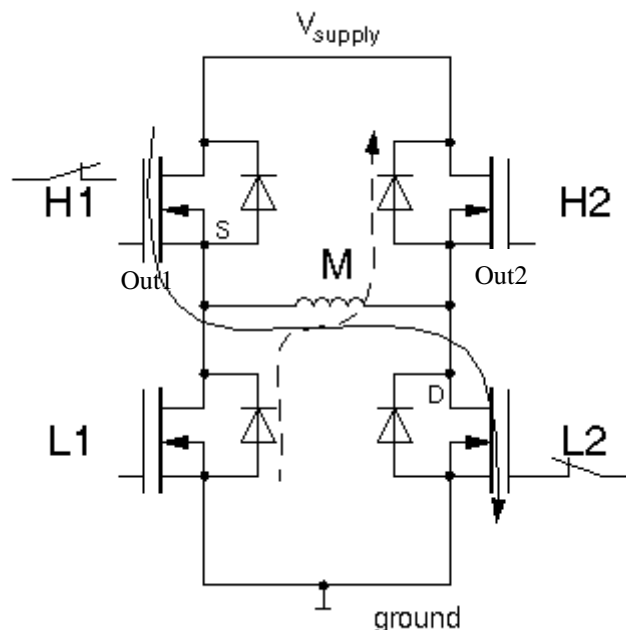
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## 1. Introduction

Control ICs for power management combine digital blocks and power stages (smart power) and work under extreme environmental conditions (automotive applications). The ESPRIT project 'SUBSAFE' studies the following design problem: When an inductive load, controlled by the smart power IC, is switched, the potential of a power stage n-well can dive below the substrate (p-type) potential. The switching periods to be considered are of the order of  $10\mu\text{s}$  and above. Under these 'below-substrate' conditions a considerable amount of electrons is injected into the substrate. Furthermore, holes can be injected through a parasitic PNP in the 'above supply' conditions. These carriers significantly risk destroying the functionality of logic components. Carriers in the substrate may be collected by a CMOS well and can induce latch-up.

As an example of an IC with a substrate current risk the SUBSAFE project investigates an H-bridge from BOSCH. This 6A H-bridge is designed for the control of DC and stepper motors in safety critical applications. Fig. 1 shows a schematic circuit of the H-bridge. The bridge consists of four LDMOS (Lateral Double diffused Metal Oxide Silicon) power transistors.



*Fig. 1 : Schematic circuit of the H-bridge. Additionally the bulk-drain diodes are drawn.*

To achieve a current flow through the motor M (represented by an inductance), either the LDMOS transistors H1 and L2 or H2 and L1 are switched on. For a closer look at the switching behaviour, we assume that H1 and L2 are switched on. For the following discussion, H2 and L1 will be looked as switched off ( $V_{\text{GS}}=0$ ). Therefore, as a starting point, DC current flows through the motor as represented by the solid arrow in Fig. 1. If H1 and L2 are switched off, the motor inductance maintains the current direction for a certain time; the only possible current path is from ground through the parasitic diodes of L1, the motor and the body-drain diode of H2 to supply (dashed arrow). Because of these forward biased diodes,

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the drain potential of L1 will be below ground and the source potential of H2 will be above supply voltage. Fig. 2 shows a measurement of a switching of the H-bridge.

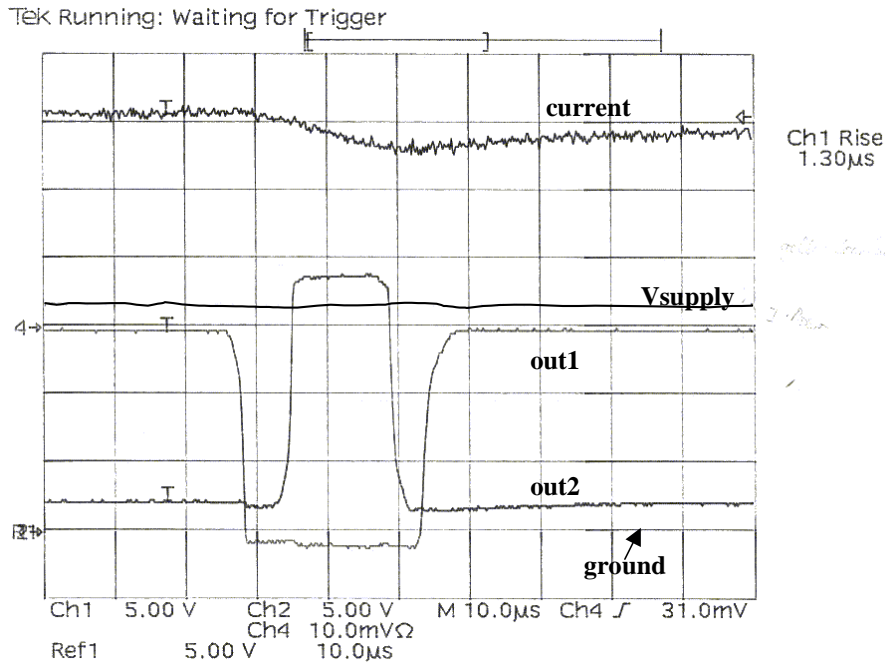


Fig. 2 Switching of the H-bridge: The ‘below ground’ of out1 and the ‘above supply’ of out2 can clearly be observed.

Fig. 3 shows a simplified cross-section through the LDMOS transistors L1 and H2. When the drain diffusion of L1 (n-well) dives below ground, electrons are injected into the substrate. These electrons either recombine with holes in the substrate or they are collected by another n-well (parasitic NPN effect). At the same time the source diffusion of H2 is driven above supply. The p-body contact of the source injects then holes into the n-epi and n-buried layer. Most of the holes recombine there with electrons, but some reach the substrate (parasitic PNP effect).

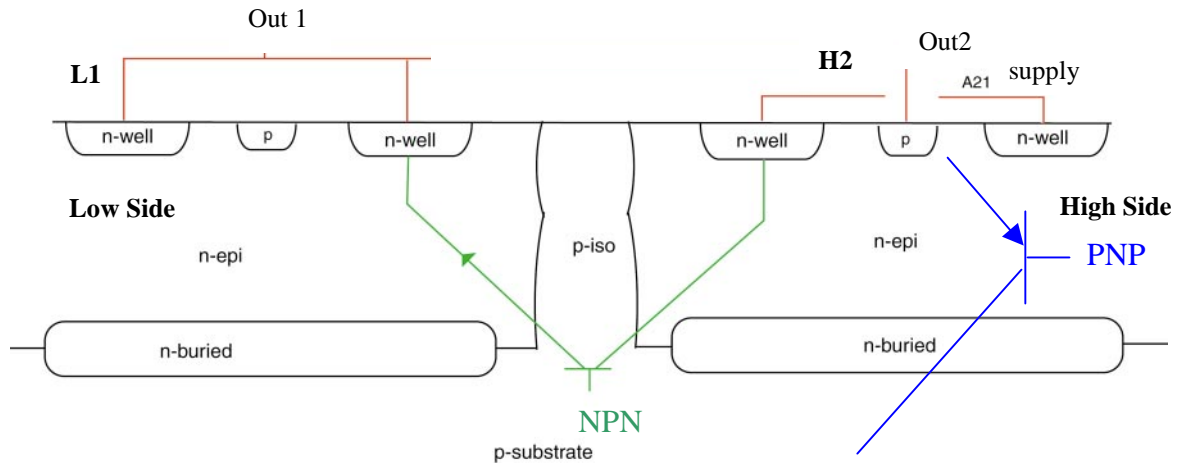


Fig. 3 Simplified cross-section of the LDMOS transistors L1 and H2 with the two parasitic transistors. The NPN injects electrons and the PNP holes into the substrate.

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The substrate currents injected by parasitic power stage transistors are low frequency currents (with switching times of the order of  $\mu\text{s}$ ) and of considerable amount (hundreds of mA). This can lead to potential shifts around one volt in the substrate. This is quite different from the substrate noise problem where noise originating from fast switching digital devices shows peak values of a few hundred millivolts. Most of the noise current flows near the surface of the substrate and guard rings are therefore appropriate to shield sensitive components.

Until now it has been state of the art to deal with the substrate current design risk on an empirical basis using general recommendations extracted from earlier experience. TCAD (Technology Computer Aided Design), the physical simulation of the underlying phenomenological partial differential equations (Poisson, electron and hole continuity, etc.) on a grid, provides a valuable complement to experiments and measurements. Computer experiments have a fast turnaround time and permit to “look into devices” in ways that are not accessible to measurements.

In the following, an overview of first simulations of the substrate current issue shall be given.

## 2. The Mesh<sup>1</sup>

The physics of semiconductor devices is described by tightly coupled non-linear partial differential equations (PDEs). The semiconductor PDEs are difficult to solve due to the high degree of non-linearity involved. The PDEs must be solved with appropriate boundary and initial conditions over the device domain. No closed-form solutions exist, and therefore only approximated solutions can be obtained. These solutions are computed by simulating a discrete representation of the PDEs over a spatial decomposition of the geometry of the device. A *mesh* is required. A mesh is a spatial decomposition of a geometric domain into simple elements, usually triangles/tetrahedrons. When computing approximate solutions, the transfer of qualitative properties from the PDEs to the discrete systems is critical. Major concerns are the stability of the solution and the accuracy together with an acceptable computing time and memory consumption. Therefore, the mesh has to be well adapted, i.e. its elements should be refined in regions where high errors in the solution and large gradients of important variables (doping, electric field, etc.) are expected. Fig. 4 shows an example of a not adapted (left) and a well-adapted mesh at a junction.

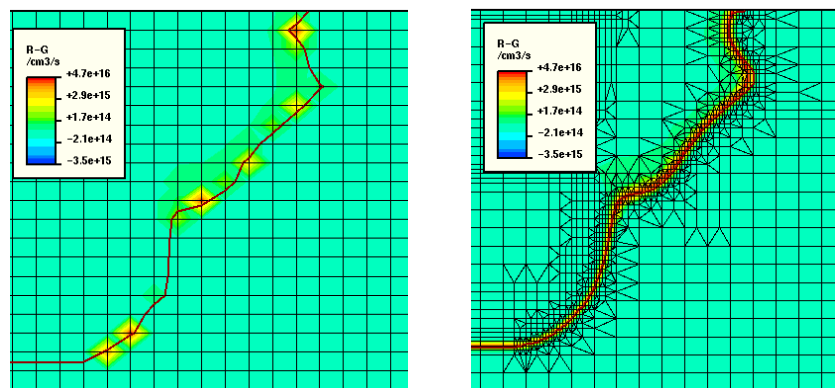


Fig. 4 The recombination current at a forward biased junction is strongly dependent on the mesh.

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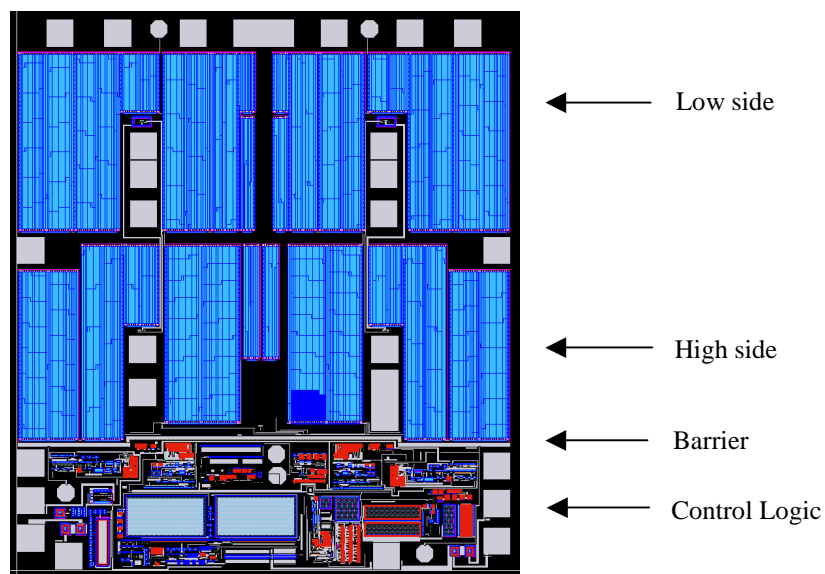
With the not adapted mesh the recombination current at the junction cannot be calculated correctly.

*Conclusion:*

Only with a problem specific adaptation of the grid a sufficiently accurate simulation is possible within reasonable calculation times.

### 3. Topology Reduction

The layout of the H-bridge chip is by far too complex as that the whole chip could be simulated with a device simulator. Fig. 5 gives an idea of the complexity of the chip. Four power stage LDMOS transistors (in the upper part of the chip) occupy almost the whole chip and only a small part at the bottom contains the complex logic controlling circuitry. The logic part is guarded from influences of the power part by a ‘barrier’ consisting of a  $p^+$  diffusion that is connected to ground.



*Fig. 5 Top view of the H-bridge chip: The four power stage transistors in the upper part and the control circuitry in the lower part can clearly be seen. The size is about 3.7mm x 4.1mm.*

Due to the complexity, the structures have to be simplified to the most important parts. Complex parts can sometimes be replaced and modelled by a simple combination of diffusions and contacts. One of the main issues in this project is a simple but accurate modelling of the injection of electrons and holes in the substrate during the switching of the H-bridge. As an example the topology reduced LDMOS for the parasitic NPN effect shall here briefly be described. The power stage LDMOS transistors consist each of about 120 fingers of parallel transistors. The whole array lies in an n-epi and under the epi an n-buried layer was implanted. A sinker surrounds the structure and connects the buried layer. Fig. 6 illustrates this: 24 fingers of one power stage LDMOS transistor are shown.

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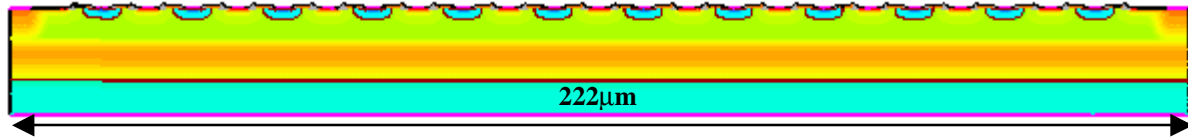


Fig. 6 Doping information of the real LDMOS transistor consisting of 24 parallel fingers.

During the activation of the parasitic NPN all drain diffusions (n-wells) dive below ground. As a consequence also the n-epi and the n-buried layer see the negative potential and electrons are injected from the buried layer into the p-substrate. The idea for the topology reduction was therefore to model the electron injection by a contact on top of the n-epi and buried layer, neglecting all n-wells and p-body diffusions, gates and oxides of the real LDMOS transistor. Fig. 7 shows the reduced structure:



Fig. 7 Topology reduced doping profile of the LDMOS for the study of the parasitic NPN transistor. From the real structure only n-epi, sinker and buried layer are left.

One of the main goals of this project is the full-chip simulation of the substrate current. Such a simulation is only feasible if the default mesh is very coarse and junction refinement is moderate. Even then, the 3D-mesh of the full chip consists of more than 25'000 vertices. The solution of the Poisson, electron and hole diffusion equations on this mesh needs about 1Gbyte of memory.

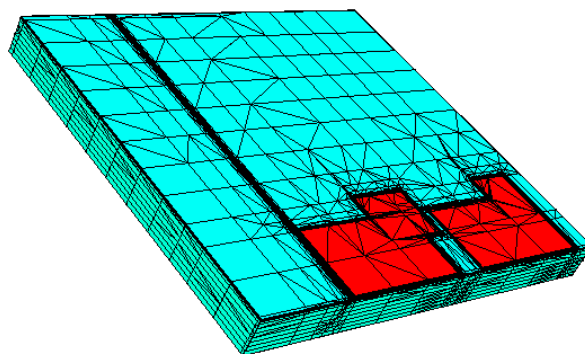


Fig. 8 Shows the simplified H-bridge with two power stages (red). The chip size is approximately (4.8mm x 4.4mm x 0.4mm).

**Conclusion:**

In order to perform a simulation on full chip level, the structure has to be simplified. This simplification, called topology reduction, has to be defined both for the power stages and for the digital part. This chapter presented topology reduction of a power stage.

#### 4. Calibration of the Device Simulator DESSIS

One of the most important advantages of TCAD is its predictive capability. But predictive TCAD and accurate results are only possible if the software tools are calibrated.

Why is a calibration necessary? The answer is: The physical equations that are solved by the device simulator on the mesh depend on material parameters. Such parameters for instance are minority carrier lifetime, mobility and doping concentration. These parameters are a priori only roughly known and must therefore be calibrated. The procedure was the following: First the fabrication process was simulated and 1D-doping profiles were calibrated using spreading resistance measurements and SIMS profiles. Then, simple structures (i.e. resistor, NPN transistor) were built with the 1D profiles and simulated with the device simulator DESSIS. The simulations were then compared to measurements of these structures performed on a testchip. Fitting the simulations to the measurements led to the unknown parameters. Fitting applies to the extraction of material parameters within a physical plausible range (no fitting by values which are orders of magnitude off). Therefore this procedure is justified and is state of the art.

##### *Calibration of the Substrate Doping Concentration*

The focal point of SUBSAFE is the substrate: the distribution of carriers and potential in the substrate and over the whole chip has to be measured and simulated. For the simulation of the parasitic transistors and of the potential distribution on the chip, an accurate knowledge of the substrate doping is crucial. However, due to the minor role of the substrate doping for the functionality of the IC, the exact concentration is not known. (The wafer spec says that the doping should be between  $3.8E15\text{cm}^{-3}$  and  $8.5E15\text{cm}^{-3}$ .) The wafer doping was estimated in the following way: The ohmic behaviour between two  $p^+$  diffusions in the p-substrate (barriers) was measured and simulated. The two barriers had a distance of about  $260\mu\text{m}$  and were about  $2760\mu\text{m}$  long. Due to the length to width ratio a 2D simulation was possible. Between the barriers a buried layer/n-epi/n-well was diffused. The left side of Fig. 9 shows the simulated hole current distribution.

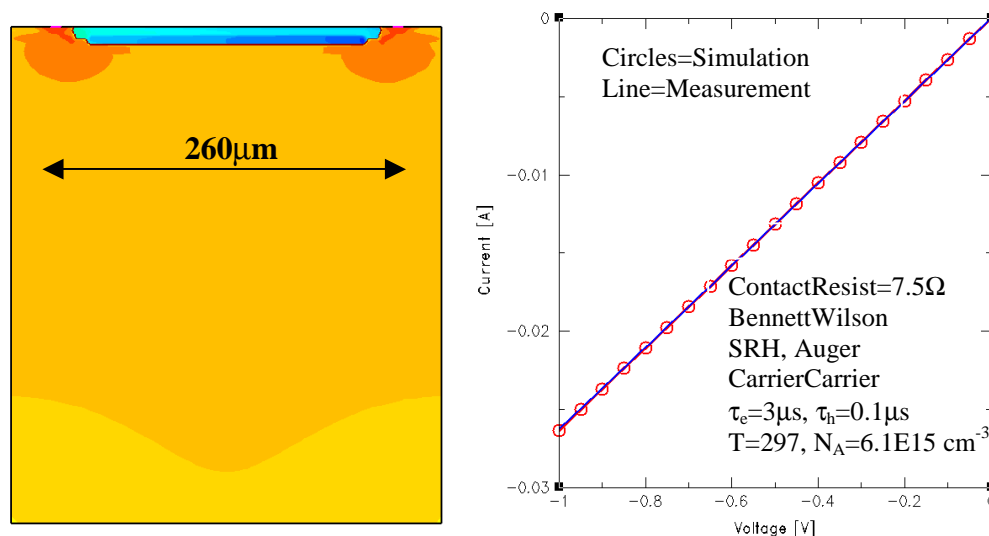


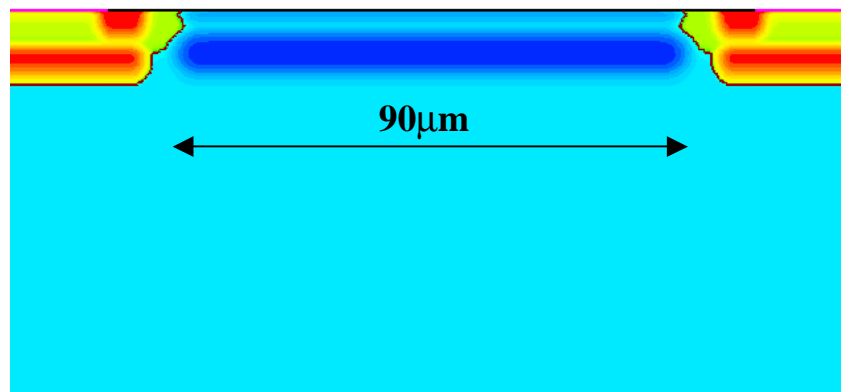
Fig. 9 Simulated hole current distribution between the two barriers and comparison with measurement.

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Holes enter at one contact into the substrate and flow under the buried layer to the second contact. The main parameter influencing this is the doping of the substrate. Therefore the doping in the simulation was changed until the simulated and the measured currents agreed. The right side of Fig. 9 shows a comparison between the measured current (blue line) and the simulated values (red circles). A substrate doping of  $6.1E15\text{cm}^{-3}$  was estimated. This value lies within the specification of the wafer doping.

*Calibration of the Electron Lifetime*

The authors suppose that the electron lifetime in the p-substrate is the most important and not well-known parameter for the simulation of the substrate current distribution. The recombination time of electrons in the p-substrate was estimated comparing measurement and simulation of a parasitic NPN-transistor built by two power stage LDMOS transistors (compare with Fig. 3, Fig. 5 and Fig. 10).



*Fig. 10 Doping profile of the parasitic NPN transistor: Emitter and collector consist of the contacts, sinker, n-epi and n-buried layer at the left and right boarder of the picture. The base is built by the p-substrate and the isolation between the two n-wells.*

The drain of the left (low side) LDMOS acts with its n-plus/n-epi/n-buried layer as the emitter, the drain of the right (high side) LDMOS acts with its n-plus/n-epi/n-buried layer as the collector and the p-substrate, which was connected through a  $p^+$  barrier contact, is the basis of the transistor. The lengths and widths of the emitter and collector blocks are about  $930\mu\text{m}$  and the length of the barrier contact is about  $2760\mu\text{m}$ . To treat a realistic situation the drain of the left LDMOS was ramped from  $0\text{V}$  to  $-1\text{V}$ , the drain of the right LDMOS was held at  $14\text{V}$  and the barrier was connected to  $0\text{V}$ . During the measurement of this structure the backside of the wafer and the source and gate contacts of the two LDMOS were not connected. In the next step, the structure was simulated in 2D and the electron recombination time was fitted to the measurement.

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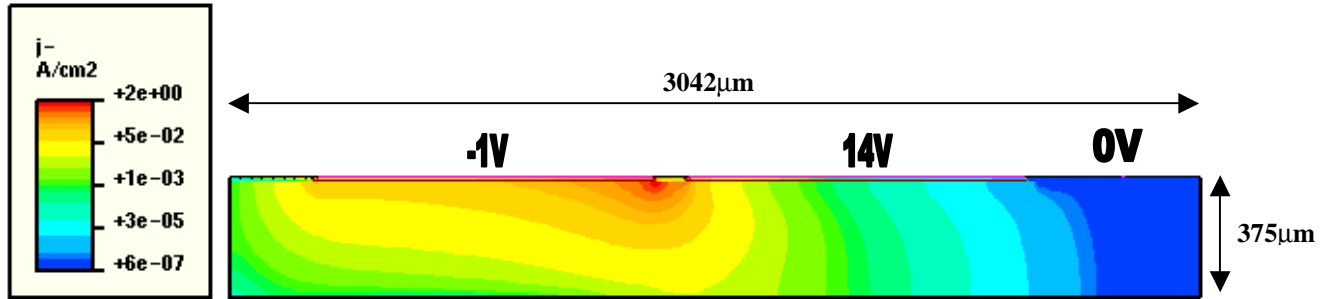


Fig. 11 Electron current density distribution of the parasitic NPN.

Fig. 11 shows the simulated electron current density with  $\tau_e = 3\mu s$ . The emitter was at -1V, collector at 14V and substrate at ground. It can clearly be seen that the electron concentration reduces quickly. This is due to the relatively small diffusion length of the minority carriers in

the substrate  $L_n = \sqrt{D_n \cdot \tau_n} = \sqrt{\frac{kT}{q} \mu_n \cdot \tau_n} \approx 100\mu m$ .

The problem with the 2D simulation (described above) is that the barrier contact (base) width is about the double of the emitter and collector width. The structure is therefore not really 2D. In this section, the 2D simulation shall be compared with a 3D simulation of the two n-wells and the barrier contact. Fig. 12 shows the substrate potential distribution. The low side (emitter) lies at -1V and electrons are injected into the substrate. The high side (collector) lies at 14V and the barrier = substrate contact (basis) is at 0V.

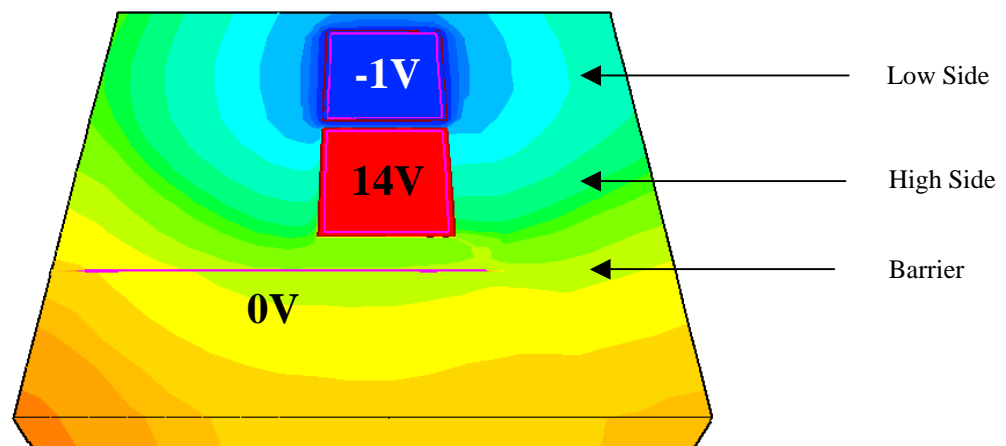


Fig. 12 Simulated distribution of the substrate potential on the testchip.

Fig. 13 compares measurement and 3d-simulation of the parasitic NPN-transistor.

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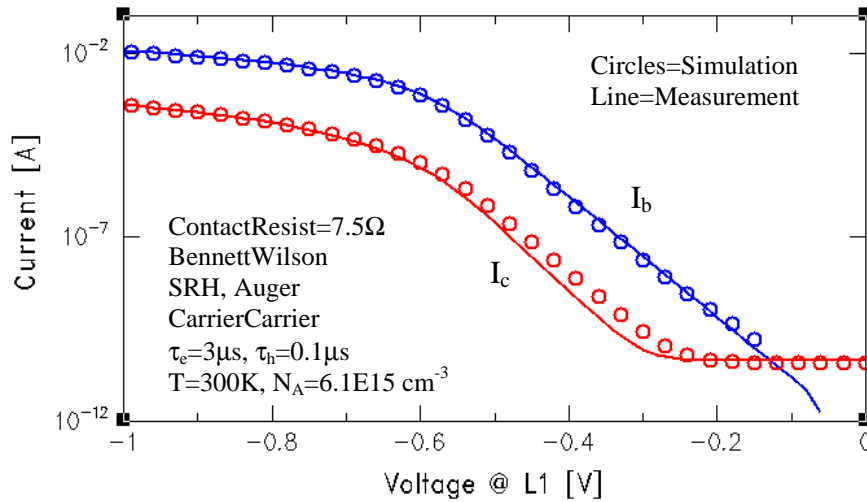


Fig. 13 Comparison of measurement and 3d-simulation of the parasitic NPN-transistor.

The collector current of the parasitic NPN transistor reacts very sensitive on the value of the electron lifetime. Fig. 14 illustrates this fact. The parasitic NPN is therefore qualified for the determination of the electron lifetime.

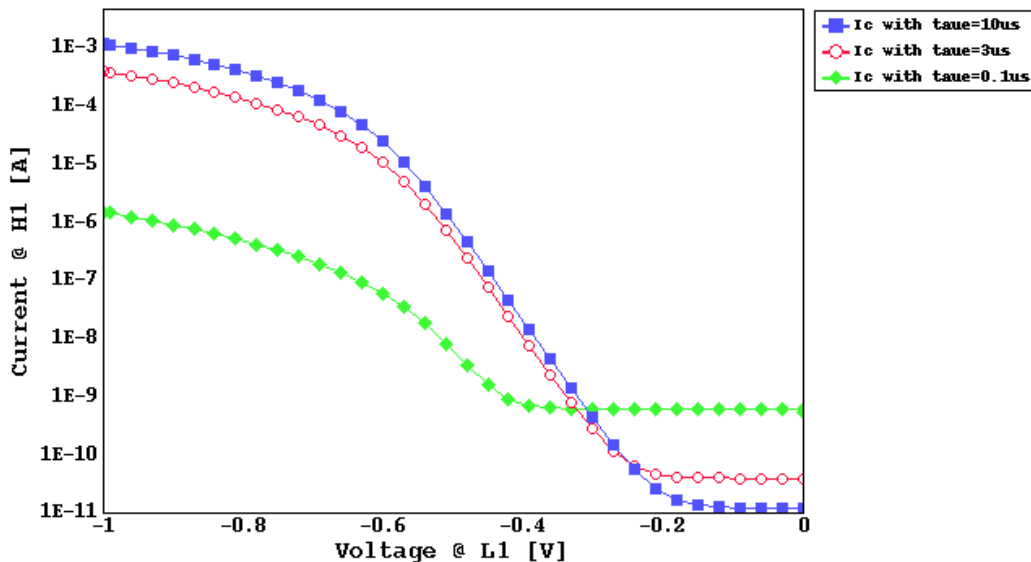


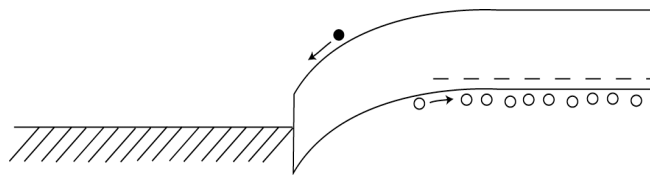
Fig. 14 The collector current of the parasitic NPN transistor depends very sensitively on the value of the electron lifetime in the p-substrate.

Conclusion:

The most important parameters for device simulation calibration are substrate doping concentration and minority carrier (electron) lifetime. Substrate doping was determined by a substrate resistance measurement. Minority carrier lifetime was deduced from a lateral NPN structure with the substrate as the base of the transistor. The collector current was measured and compared to a simulation. It was shown that the collector current depends in a sensitive way on the minority carrier lifetime.

## 5. The Schottky Contact at the Backside

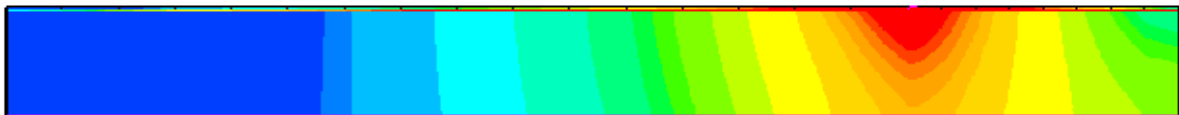
The H-bridge chips are metallized with chrome at their backside. Therefore, the backside contact is a Schottky contact. The type of the backside contact is believed to be very important for the substrate potential shift induced by substrate current. When the potential at the drain contact of the low side is driven below the substrate potential, electrons are injected into the substrate. Depending on their diffusion length, these minority carriers either recombine with holes or they diffuse to the backside contact or to the high side or even into the logic part. A good backside contact should deliver enough holes for recombination and should be a good sink for electrons. After electron injection the substrate potential becomes in any case negative with regard to the potential of the backside. This means, however, that the Schottky diode becomes reversed biased. The bands of the silicon bends then in the vicinity of the backside contact in the following way (see Fig. 15):



*Fig. 15 Schematic of the reversed biased Schottky diode at the backside.*

For electrons the Schottky diode is a good sink, holes, however, cannot be delivered by the metal-semiconductor contact. Therefore, the minority carriers have to either diffuse through the whole wafer to the backside contact or the n-doped regions of the high side (parasitic NPN) can collect them or they can recombine with holes delivered from the barrier contact. In any case the distribution of the electrons becomes wider.

An accurate description of the backside contact is crucial for a good simulation of the substrate current distribution. It must therefore be included in simulations of the potential distribution in the substrate. Fig. 16 shows a 2D simulation of the hole current flow from the barrier contact to the backside.



*Fig. 16 Current flow between the barrier contact and the backside contact.*

Though the barrier contact is quite small, Fig. 16 shows a wide hole current flow through the chip. One reason is that the structure was simulated with only p-type bottom-isolation at the top. Holes disperse therefore from the barrier contact at the top over the whole surface. In reality the hole flow is limited at the surface by adjacent n-wells and n-buried layers. In spite of that the simulation gives quite a good fit of the measured current flow through the chip. This is compared in the Fig. 17:

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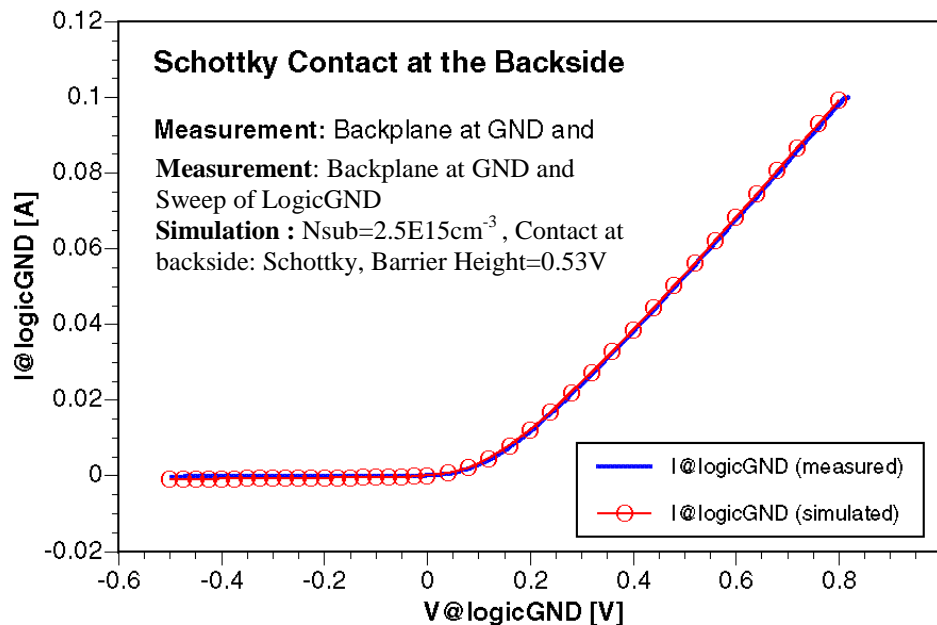


Fig. 17 Comparison of measurement (line) and simulation (circles) of the Schottky barrier at the backside.

The Schottky barrier height was used as fitting parameters. 0.53V was chosen as barrier height. This value is comparable with the measured Schottky barrier height of 0.5V between chrome and p-type silicon (see Sze, “Physics of Semiconductor Devices”, Wiley 1981, p. 291). Finally, it should be mentioned that the grid has a strong influence on the best fit for the Schottky barrier. Therefore, refinements of the mesh are necessary not only in the active layer, but also at the backside.

*Conclusion:*

In power applications chips are often contacted via the backside. This backside contact is normally a Schottky contact, which strongly influences the electrical behaviour of the substrate. The backside contact can be well described by device simulation. The relevant parameter to be calibrated is the Schottky barrier height.

**6. Static Simulation of the Potential Distribution**

When electrons at the low side are injected into the substrate the potential in the substrate shifts to negative values. The shift hardly depends on the voltage at the high side. This is due to the fact that only a small part of the injected electrons reach the high side, but most of them recombine earlier. To simulate a realistic situation at the low side a potential of -1V was applied, the backside contact was held at ground and the high side at 0.4V. The small high side voltage was chosen to accelerate the simulation and to reduce the colour scale of the picture. (In a real application the voltage on the high side would be about 14V.) Fig. 18 shows

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the calculated potential distribution in the substrate. (This figure presents a vertical cut through the structure presented in Fig. 12.)

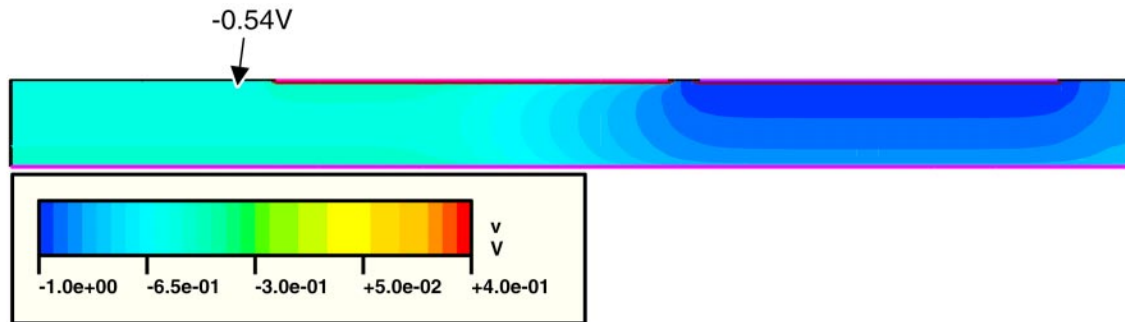


Fig. 18 Substrate potential distribution when at the backside a Schottky barrier ( $\Phi=0.53V$ ) is assumed and at the low side  $-1V$  is applied.

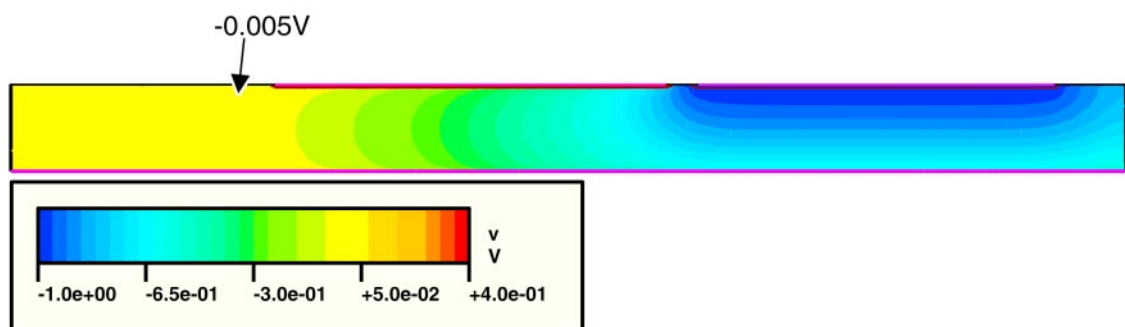


Fig. 19 Substrate potential distribution when at the backside an ohmic contact is assumed and at the low side  $-1V$  is applied.

The crucial influence of the Schottky barrier can be seen comparing Fig. 18 with Fig. 19, which was calculated with an ohmic contact at the backside. Viewing at the potentials in the logic part, it can be seen that the substrate potential lowering is smaller in the case where a good ohmic contact at the backside exists.

The potential distribution was also simulated in 3D: The low-side n-well was first swept to  $-1V$  and then to  $-2V$  and the high side n-well was hold at  $14V$ . To the backside and the barrier contact  $0V$  were applied. The backside contact was of Schottky type with a barrier height of  $0.53V$ . The potential at various points was determined in the following way: Electrodes at various sites on the chip surface were distributed and the contacts were defined with a current boundary condition of  $0A$ . The simulation output gave then the voltages at the electrodes. They are shown in Fig. 20.

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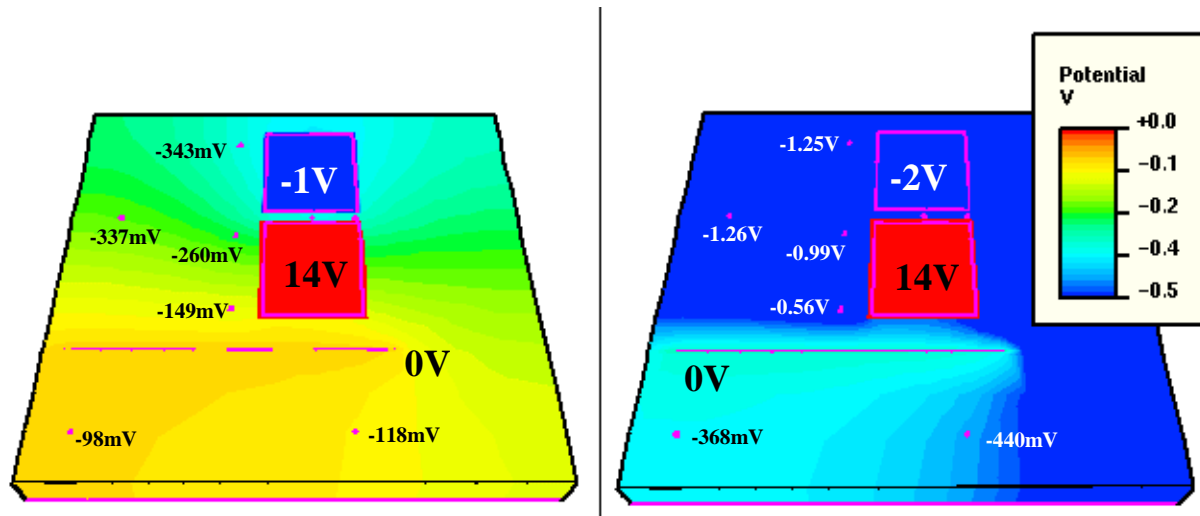


Fig. 20 3d-simulation of the potential distribution during electron injection. The n-well was ramped quasi-static to  $-1V$  (left) and then to  $-2V$  (right). The scale was cut at  $-0.5V$  in negative and at  $0V$  in positive direction.

*Conclusion:*

DC full chip simulations are feasible and show consistent results. The relevance of the Schottky backside contact was illustrated. The simulations presently serve as a basis for a validation against the measurements.

## 7. Transient Simulation of Potential Distribution

Fig. 2 showed a measurement of the switching of the H-bridge. The drain of the low-side LDMOS transistor goes in about  $2\mu s$  from  $14V$  to about  $-1V$ . A similar situation shall now be simulated: Fig. 21 shows a transient simulation of the potential distribution during electron injection. The high-side contact was ramped to  $14V$  and the barrier and the backside contact (with Schottky barrier height  $0.53V$ ) were held at  $0V$ . Then, the low side contact was swept transiently from  $0V$  to  $-2V$  and the potential distribution in the chip at different times were saved. The four pictures of Fig. 21 show clearly the effectiveness of the barrier contact: The potential shift behind the barrier where the logic circuits are placed is considerably smaller.

Furthermore, it was supposed that in transient mode the potential shift would be by far higher than in quasi-static situation. This is, however, not true. The negative potential shift is of the same order of magnitude as in the case of the quasi-static ramp (compare the right picture of Fig. 20 with the potential distribution at  $-2\mu s$  shown in Fig. 21).

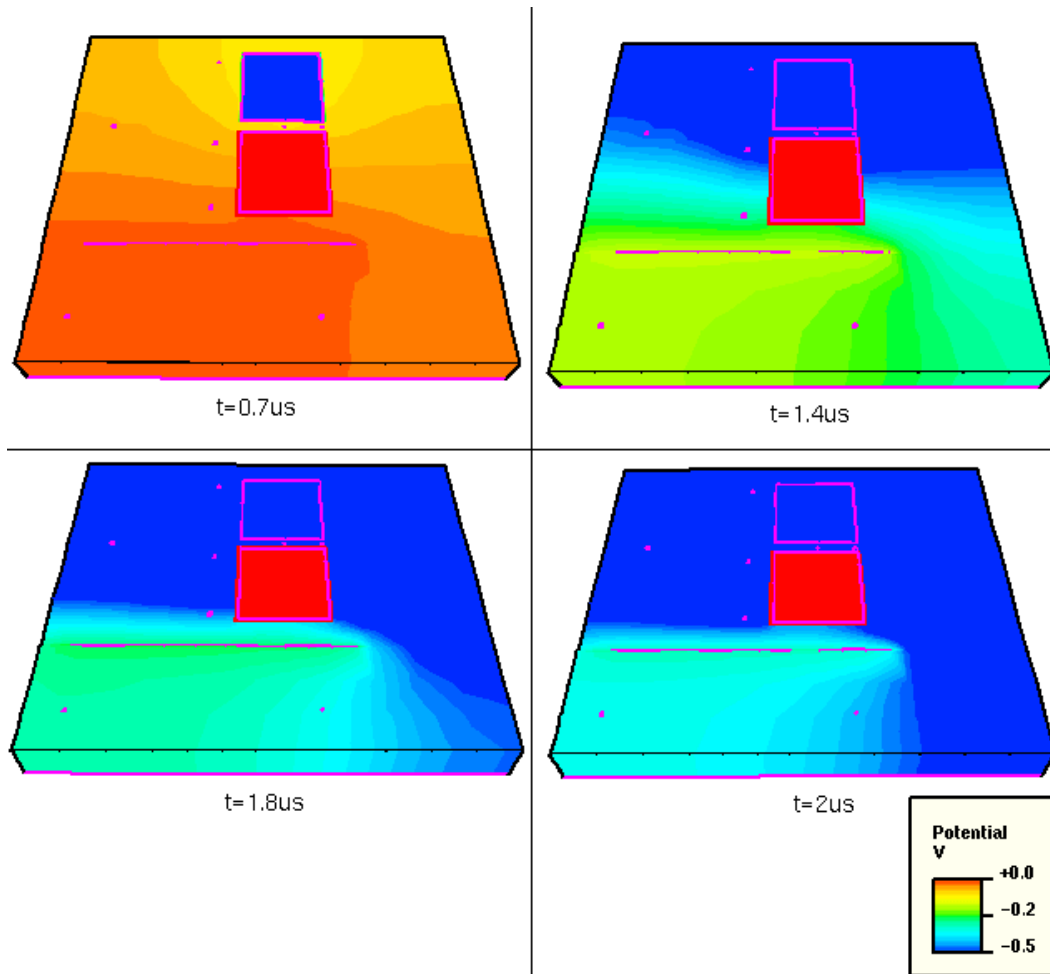


Fig. 21 Transient simulation of the potential distribution during electron injection. The n-well is ramped in  $2 \mu\text{s}$  from  $0\text{V}$  to  $-2\text{V}$ .

*Conclusion:*

In the  $\mu\text{s}$  time range the transient turn on behaviour does not significantly differ from the static behaviour.

## 8. Influence of Substrate Current on a Bipolar Device

Electrons injected at the low side of the power stage can be collected by any n-well on a positive potential. In the following section the influence of electron collection by the buried layer of a NPN device shall be studied. Geometry and doping of the NPN look as follows (see Fig. 22):

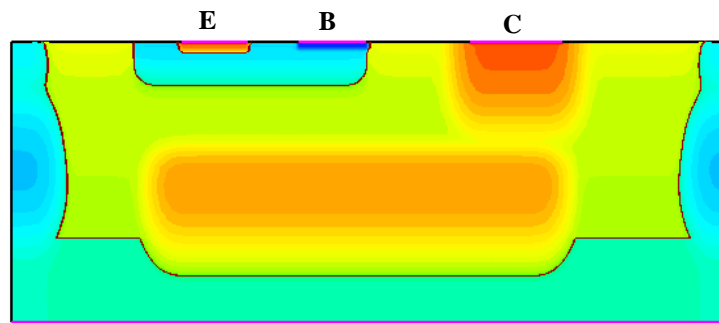


Fig. 22 *Cross-section through a NPN device.*

Fig. 23 shows the electron current distribution when the transistor is on.

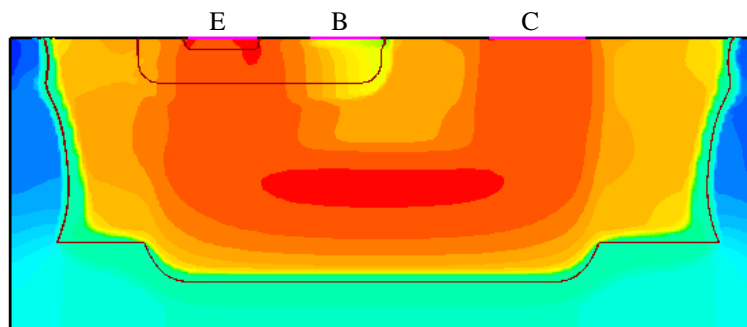


Fig. 23 *Electron Current Distribution in the NPN device.*

To study the influence of substrate current an electron source was placed nearby the transistor. Fig. 24 and Fig. 25 show the doping and the electron current distribution. The electrons from the electron source are either collected by the buried layer or they flow into the backside or recombine with holes from the substrate.

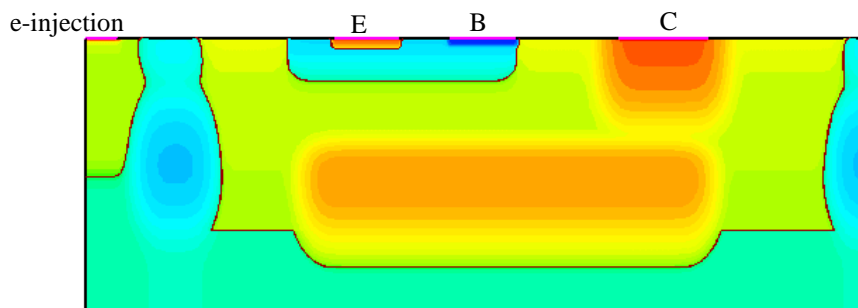


Fig. 24 *Doping profile of the NPN with an additional n-well nearby. The n-well acts as an electron source.*

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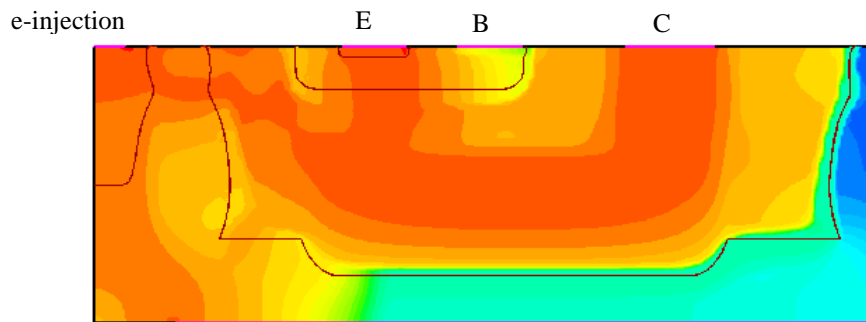


Fig. 25 Electron current distribution of the NPN device when nearby the transistor additional electrons are injected.

Fig. 26 shows the influence of the electron source on the characteristics of the NPN device. Obviously, the collector current is shifted by the injected current. In this example the influence is quite strong, but in reality, the electron source is far away and the influence will be smaller. This will be shown in the next simulation.

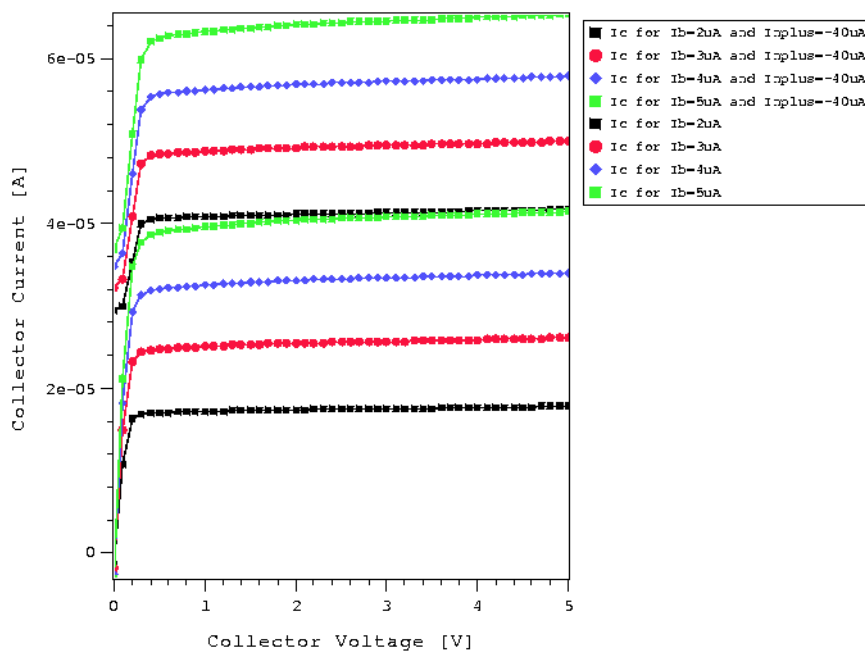


Fig. 26 The NPN characteristic without electron source (lower curves) and with electron injection ( $I = -40 \mu\text{A}$ ).

In reality, the electron injection at the low side of the power stage is far away from a NPN transistor in the logic part of the H-bridge chip. The question is: Will the functionality of such a device be disturbed by the electron injection at the power stage? Fig. 27 shows a simplified 2D cross-section with the low and high side power stage transistors and far away a NPN device.

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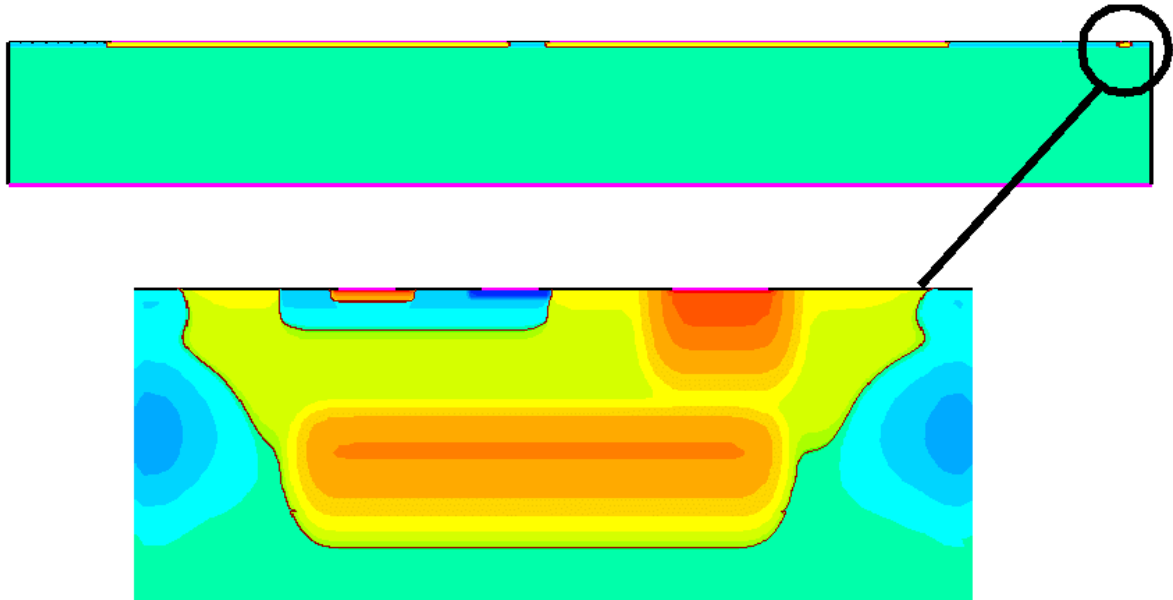


Fig. 27 Simplified 2D cross-section through the H-bridge chip (upper picture) and zoom into a NPN transistor in the logic part of the chip (lower picture).

Fig. 28 shows the simulation of the electron current distribution during low side injection. The lower pictures is a zoom into the logic part where a NPN transistor was placed. Obviously, the influence of the substrate current on the NPN transistor remains small.

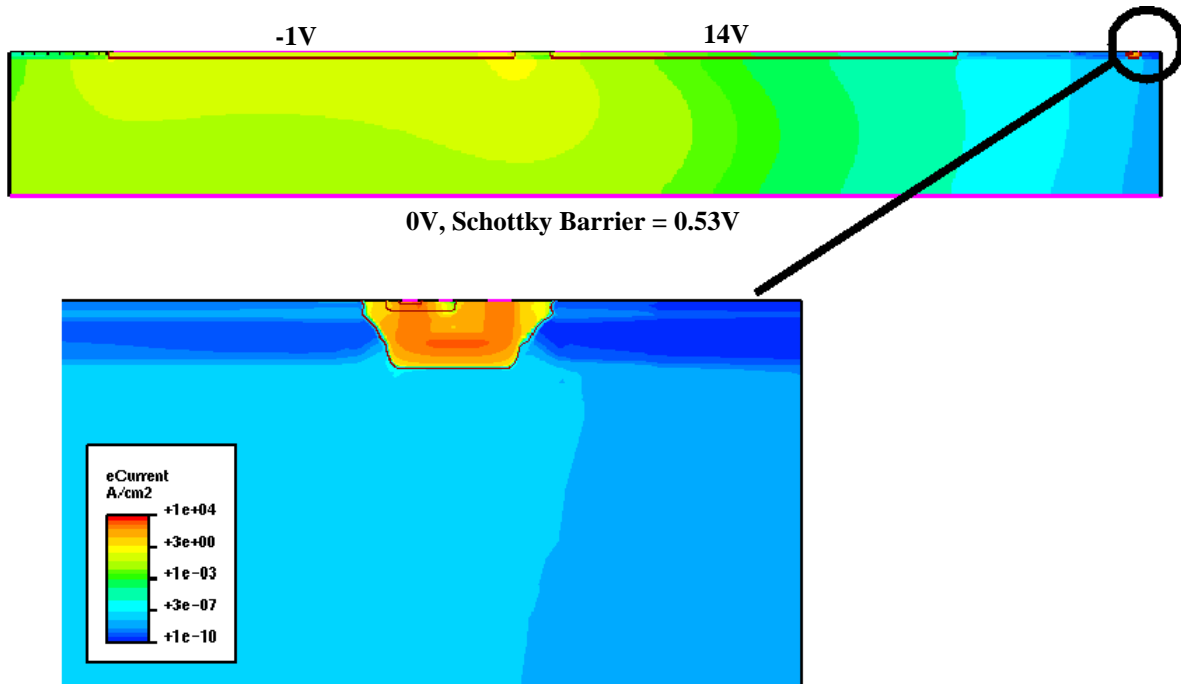


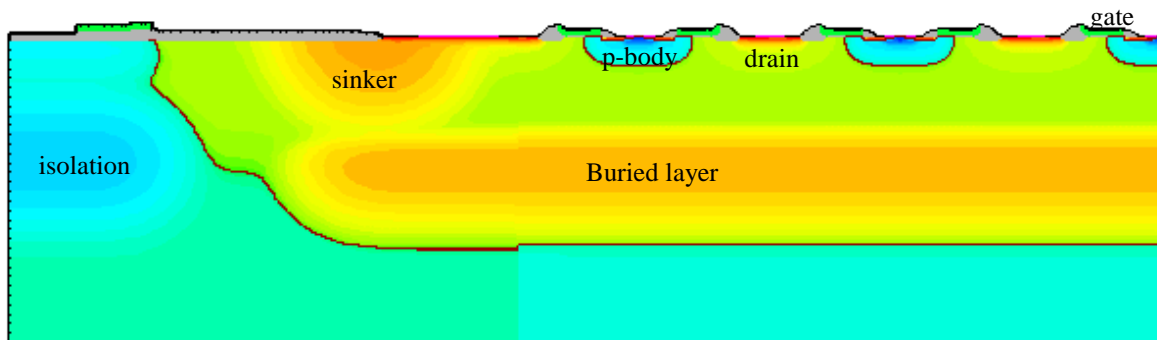
Fig. 28 Electron current distribution during low side injection. The influence of the substrate current on a NPN transistor far away is neglectible.

*Conclusion:*

If a device with a relatively small N-well (here an isolated NPN) is far away (more than 1mm) the minority carrier injection via the substrate is small ( $\ll 1\mu\text{A}$ ) and does probably not disturb the IC functionality.

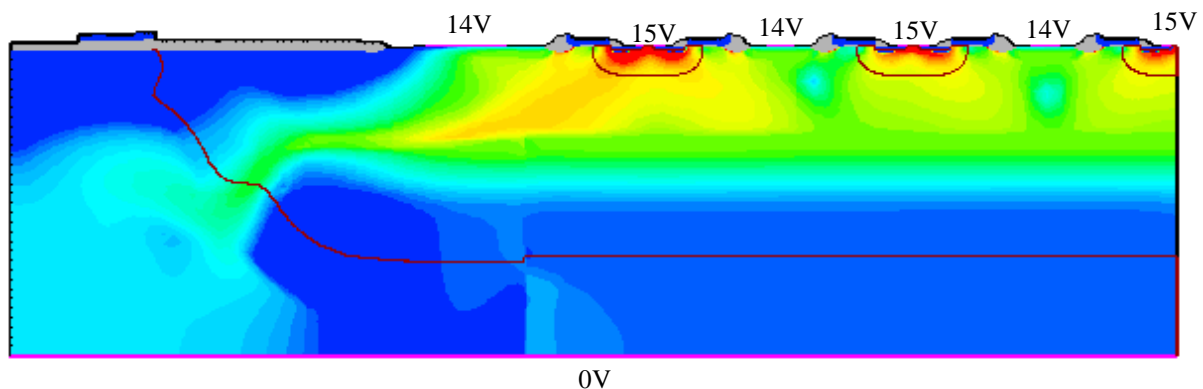
### 9. High Side Injection: The parasitic PNP Transistor

In the previous chapters only electron injection through the low side power LDMOS was considered. In the following chapter hole injection through the parasitic PNP transistor at the high side of the power stage shall be briefly studied. Fig. 29 shows a 2D process simulation of a boarder part of a LDMOS. (Unfortunately, there is a small mismatch in the substrate doping of the right side compared with the doping on the left side.) The simulation shows the sinker, the buried layer and n-epi of the LDMOS, three p-body diffusion and five poly gates.



*Fig. 29 2D process simulation of the LDMOS (there is a small mismatch in the substrate doping at the left part compared to the right part.)*

Fig. 30 shows the distribution of the hole current when the parasitic PNP is activated. A considerable part of the current flows through the boarder where the sinker/buried layer diffusion has a minimum (compare with Fig. 29).



*Fig. 30 The parasitic PNP of the LDMOS: Holes flow from the source into the substrate.*

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Then the parasitic PNP action in the whole substrate was studied: Fig. 31 and Fig. 32 show the doping and the hole current distribution of one LDMOS block in the p-substrate. Most of the holes injected by the PNP into the substrate flow directly into the backside contact.

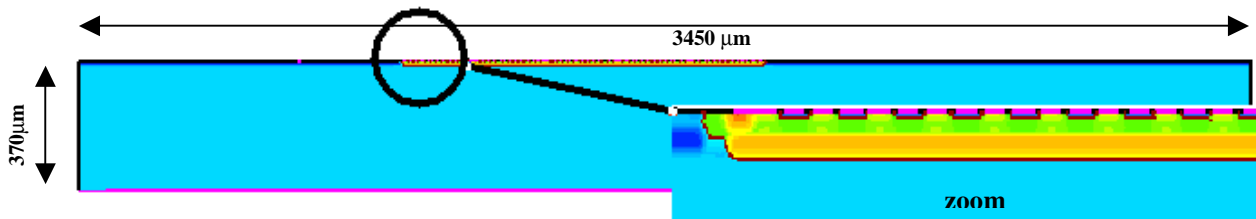


Fig. 31 Doping of the whole LDMOS block in the chip and zoom into the left boarder part.

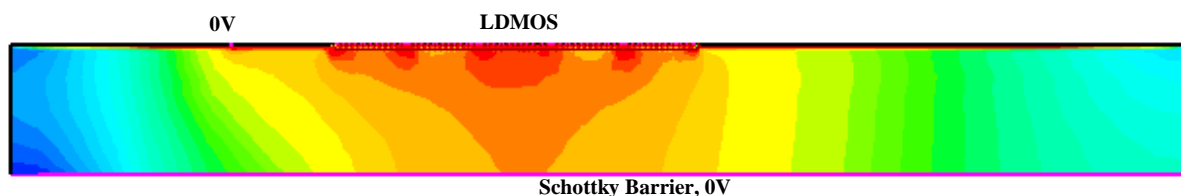


Fig. 32 Simulation of the hole current distribution when holes are injected in the substrate through the parasitic PNP transistor.

*Conclusion:*

Hole flow of the parasitic PNP occurs not only through the buried layer (vertical) but also laterally through the lower part of the sinker. Inhomogeneities of the vertical flow due to different DMOS fingers are not observed.

## 10. Latch-up

Substrate current can lead to parametric shifts in the electric characteristics of some devices in the logic part of the smart power chip. The major concern, however, is that substrate current induces a latch-up, which can lead to a catastrophic failure of the chip. The following chapter will treat the latch-up issue.

Latch-up occurs when parasitic NPN and PNP bipolar transistors form a PNPN structure.<sup>2</sup> This constitutes a thyristor (SCR), which has the ability to switch between a high impedance blocking state and a very low impedance state. Under normal operating conditions, the SCR remains in the non-conducting state and does not interfere with circuit operation. However, under certain conditions (e.g. voltage spikes), the SCR may become triggered into the conducting state and the power supply effectively sees a low impedance path to ground. Irreversible damage can then occur to the circuit.

Fig. 33 shows a cross-section of CMOS-inverter. The parasitic NPN and PNP transistors are

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cross-connected resulting in a common base-collector junction. Under active bias the collector of the PNP delivers current to the base of NPN activating a collector current of this NPN to the base of the PNP, and vice versa. Under normal CMOS operations, the base emitter junctions are not forward biased for both bipolar transistors and as a consequence latch-up is impossible. If the current gain of the two transistors and the values of the resistors  $R_{epi}$  and  $R_{pwell}$  are sufficiently high, then the circuit can be triggered by an external disturbance into a regenerative condition where each transistor keeps driving the other.

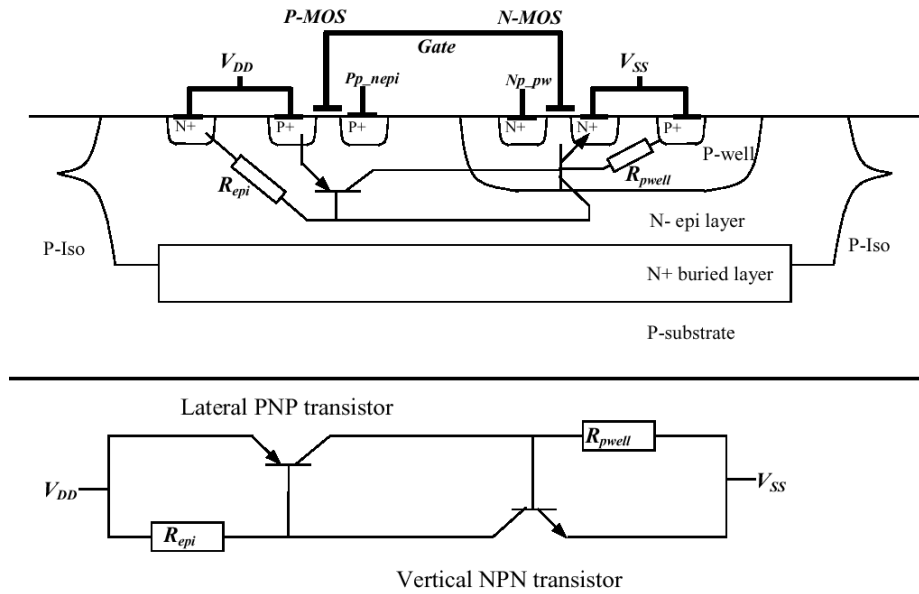


Fig. 33 Schematic cross-section of CMOS inverter structure (top) and lumped element model for the latch-up.

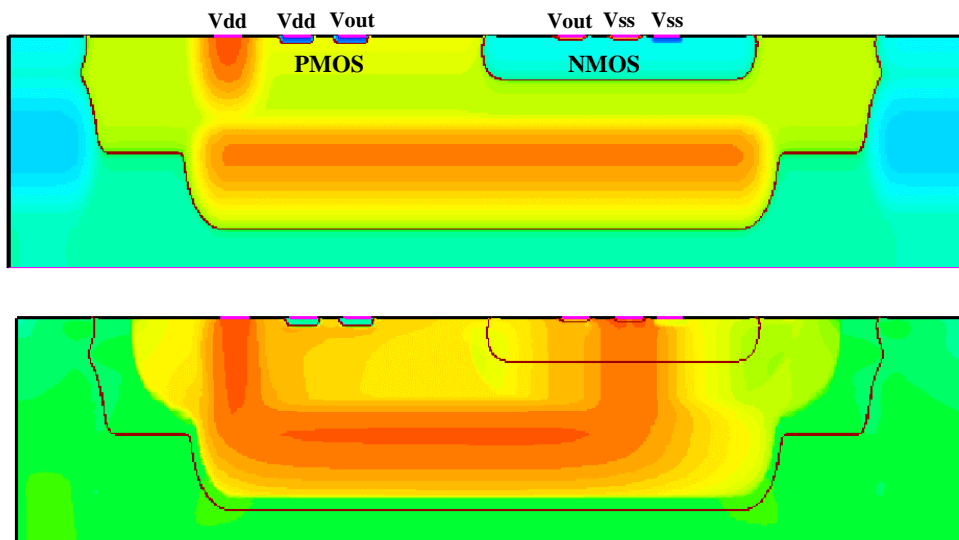


Fig. 34 2D-Simulation of a latch-up in a CMOS inverter, doping (top) and total current (bottom).

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The following section shows device simulations of latch-ups. The parasitic PNP structures are inherent in the CMOS inverter (compare to Fig. 34).

The upper picture of Fig. 34 shows the geometry and doping of a simplified CMOS inverter (without gate). The sinker contact and the drain of the PMOS were connected to  $V_{dd}$  and the source of the NMOS and the n-well contact were connected to  $V_{ss}$ . The source of the PMOS and the drain of the NMOS remained open. Then  $V_{dd}$  was ramped.

Fig. 35 shows the simulated snapback of the current when the parasitic thyristor is activated. The black curve was simulated with a distance between NMOS and PMOS of  $10\mu\text{m}$  and the red with a distance of  $22\mu\text{m}$ .

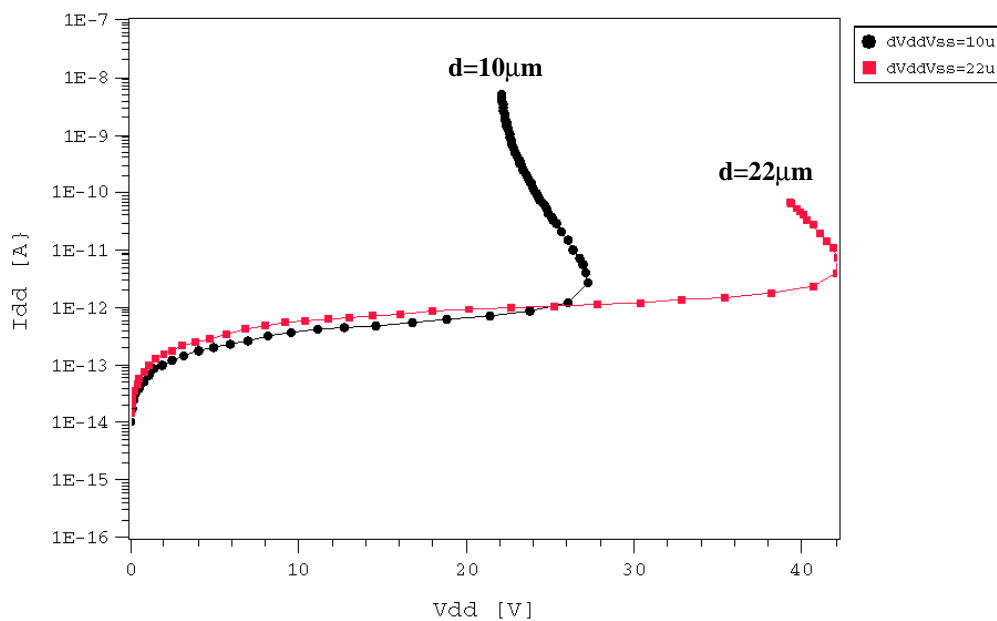


Fig. 35 Latch-up at the CMOS inverter, the forward blocking voltage depends on the distance between NMOS and PMOS.

Now, the influence of substrate current on the latch-up of the inverter shall be studied. The type of the substrate current (electron or hole) determines which transistor of the parasitic PNP structure is first activated:

#### 1) Minority Carriers in Substrate

The logic n-well serves as collector of a parasitic NPN substrate bipolar transistor. As a result electrons flow through the n-epi causing a voltage drop. This may bias the emitter/base junction of the PNP in forward direction leading to a latch-up. (Compare with Fig. 36.)

The latch-up was confirmed in a measurement on the testchip: A CMOS inverter was biased and the  $V_{ss}$  current was monitored. Then a n-well nearby the inverter was ramped to a negative voltage and electrons were injected into the substrate. The electrons were collected

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by the n-well of the inverter. Due to the voltage drop at  $R_{epi}$  the parasitic PNP structure turned on. As a result a current from  $V_{ss}$  into the substrate could be measured. This current at  $V_{ss}$  proves the latch-up of the inverter.

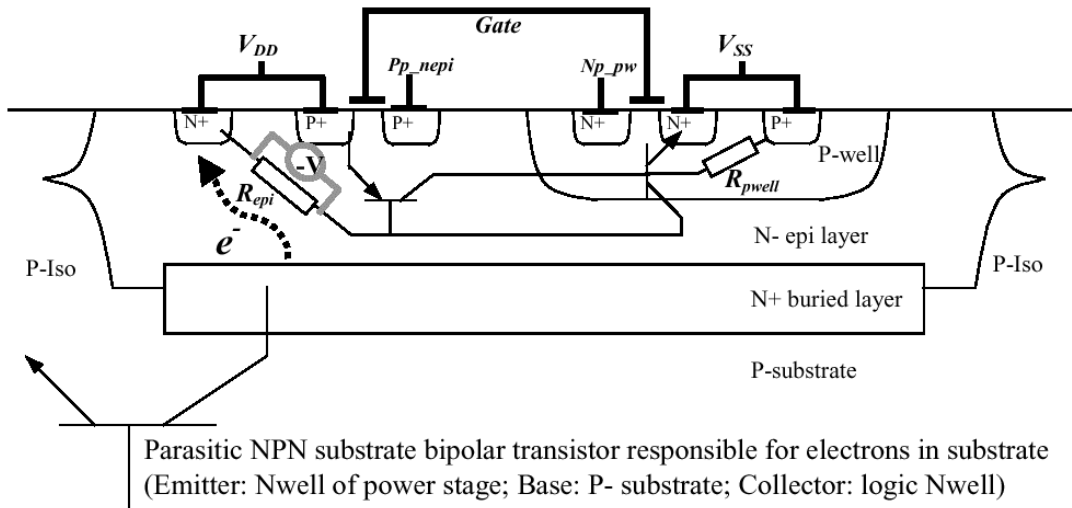


Fig. 36 Possible triggering of latch-up due to substrate electron current.

In the next step, the CMOS inverter with the electron source nearby was simulated. Fig. 37 shows the 2D-doping profile of the electron source (left) and the simplified inverter (right).

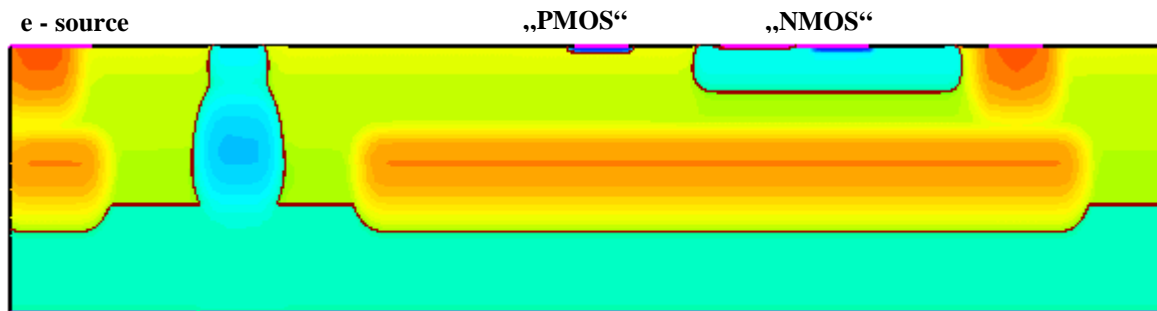


Fig. 37 Doping of the simplified CMOS inverter with a electron source nearby.

Fig. 38 shows the simulated electron distribution when the n-well at the left end of the structures is ramped to  $-2V$  and  $10V$  were applied to  $V_{dd}$ . The picture shows that the electrons either flow to the backside or they are collected by the buried layer and the sinker.

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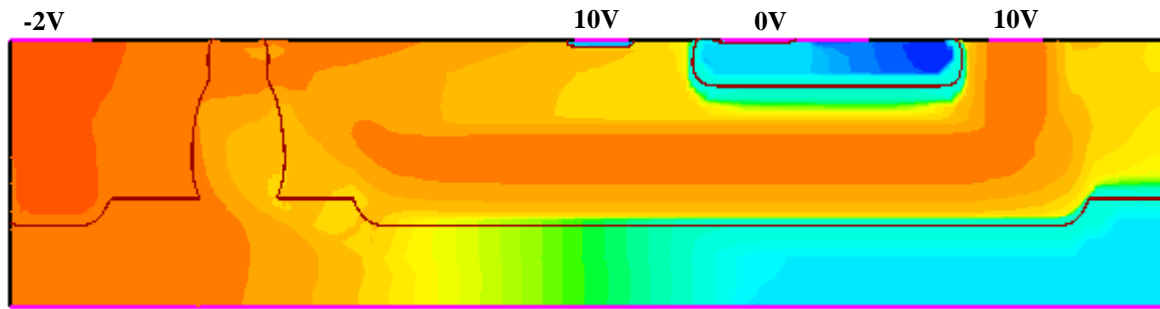


Fig. 38 Electron current distribution. Electrons are injected into the substrate (left). They are collected either by the backside or by the buried layer.

In the simulation no latch-up can be seen! In fact the actual layout of the inverter structure does not have any axis of symmetry, thus 3D effects may be relevant. The devices simulation presented above however was a 2D simulation. This difference may explain the difference from latch up simulation to measurements. Please note that simulation of the inverter structure in 3D however would, if possible, be a tremendous task. Significantly more than 100 000 vertices would be needed. Therefore, in order to continue these investigations structures appropriate for 2D evaluation have been designed on the second test chip.

II) Majority Carriers in the Substrate

A substrate current consisting of holes could also lead to a latch-up in a CMOS inverter (compare with Fig. 39): The holes have to flow through the base in order to reach the p-well. This can cause there a voltage drop and the emitter/base junction of the NPN becomes forward biased. The parasitic NPN turns on and injects electrons into the n-epi. When the electron current in the epi becomes high enough also the parasitic PNP turns on.

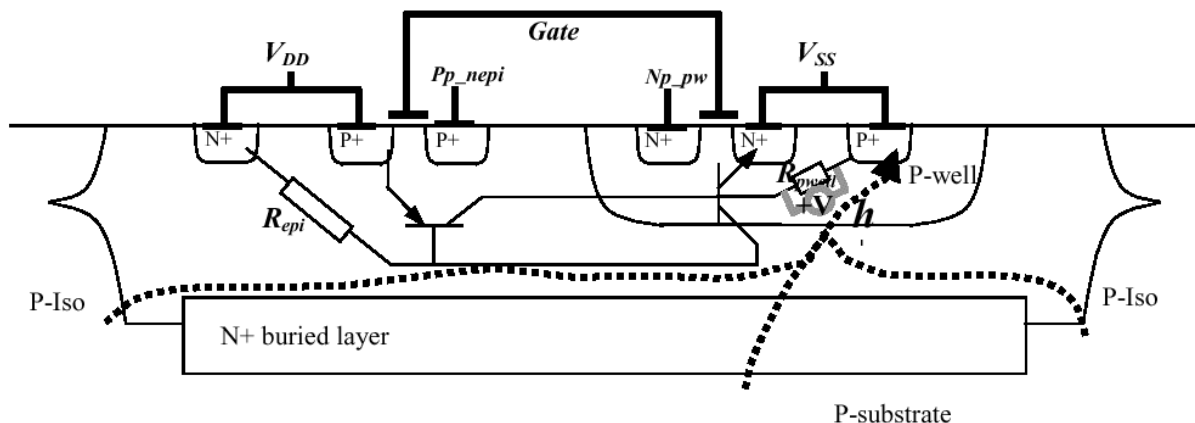


Fig. 39 Possible triggering of latch-up due substrate hole current.

As in the case of electrons the latch-up principle shown in Fig. 39 could be confirmed in a measurement on the testchip. The substrate potential was shifted by means of a substrate

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contact. Holes flowing from the substrate through the p-well into  $V_{ss}$  led to a voltage drop in the p-well. The n-plus/p-well junction got forward biased and the parasitic npn was activated. The injection of electrons into the n-epi turned on also the parasitic pnp. This mechanism was proven by measuring a current at  $V_{ss}$  flowing into the chip.

Again the situation should be explained by a simulation. Fig. 40 shows the doping profile of simplified inverter structure and in Fig. 41 the distribution of the hole current in the inverter can be observed. Unfortunately, as in the minority case, a latch-up of the structure could not be simulated. Almost all holes either flowed to the backside contact or recombined with electrons in the buried layer or n-epi. Here the same explanation as above (s. end of section *Minority carriers in the Substrate* on page 24.) applies to make plausible the differences between 2D simulation and 3D actual structure.

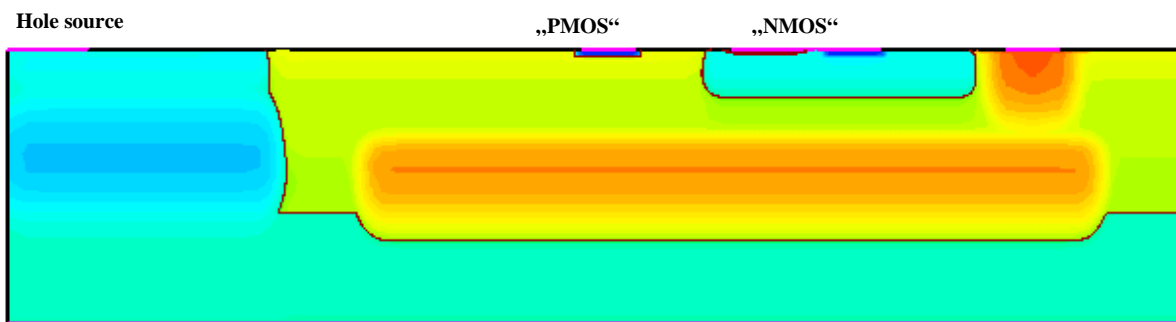


Fig. 40 Doping profile of a simplified CMOS inverter with a contact for hole injection at the left end.

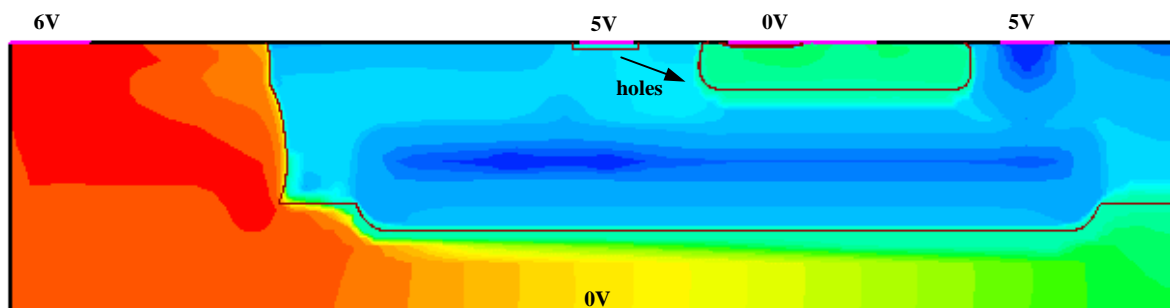


Fig. 41 Simulation of the hole current distribution. Only a small hole current from the PMOS into the n-well can be observed.

## **11. Overall Conclusion**

All relevant steps for device simulation investigation have been carried out on relevant structures and been explained. These are calibration, meshing, topology reduction and simulation application. Various simulation runs on smaller structures and on full chip level were performed. These show the importance of minority carrier lifetime, backside Schottky contact and problem specific topology reduction. This latter topic was successfully applied to simplify a power stage while approximation of a 3D inverter structure (i.e. with strongly asymmetric layout) by 2D simulation showed differences in latch up measurement and simulation.

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<sup>1</sup> Gilda Garreton, „A Hybrid Approach to 2D and 3D Mesh Generation for Semiconductor Device Simulation“, Hartung-Gorre 1999

<sup>2</sup> R. R. Troutman, „Latchup in CMOS Technology. The Problem and Its Cure.“, Kluwer Academic Publishers, 1986