

## **Deliverable D1.1.1**

# **Analysis of major nonidealities of multibit oversampling converters**



**K.U. Leuven**  
**ESAT – MICAS**

K. Francken  
G. Gielen

# Table of Contents

<b>1. Introduction</b>	<b>1</b>
<b>2. Classification of the nonidealities</b>	<b>2</b>
<b>3. Integrator related nonidealities</b>	<b>3</b>
3.1. Finite operational amplifier gain	5
3.2. Finite operational amplifier GBW	6
3.3. Non-zero switch resistance	7
3.3.1. Instantaneous OTA settling	7
3.3.2. Frequency limited OTA	8
3.4. Amplifier finite output swing	9
3.5. Amplifier slew rate limitation	9
3.6. Amplifier gain nonlinearity	11
3.7. Nonlinear switch resistance	11
3.8. Capacitor mismatch	11
3.9. Capacitor nonlinearity	12
<b>4. Comparator related nonidealities</b>	<b>12</b>
4.1. Comparator offset	12
4.2. Comparator hysteresis	13
4.3. Comparator offset and hysteresis combined	14

<b>5. Other nonidealities</b>	<b>14</b>
5.1. Clock jitter	14
<b>6. DAC nonlinearity</b>	<b>15</b>
<b>7. Conclusions</b>	<b>16</b>

## 1. Introduction

The oversampling and noise shaping techniques combined with digital filtering used in  $\Delta\Sigma$  converters allow to trade resolution in time for resolution in amplitude. As a consequence, these converters are relatively insensitive to circuit nonidealities. The success of  $\Delta\Sigma$  modulators is primarily due to the fact that current VLSI technologies are optimized for digital circuits, and consequently the trade off between digital signal processing and analog precision becomes more attractive.

In order to design a complete  $\Delta\Sigma$  modulator we can observe the following three major tasks [1]:

- Topology and accompanying topology parameter selection (crucial for performance)
- Analysis of the impact of nonidealities on the system performance and specification of the resulting building block performances
- Design, optimization and simulation of the building blocks followed by a layout of the complete system and performance evaluation

This report will concentrate on the second step, more precisely the impact of nonidealities on the system performance.

When real circuits are used, the behavior of the converter will deviate from its ideal one. Therefore an estimate of these circuit nonidealities is needed. One needs to know the impact on the performance at the system level because of different reasons. First of all this information will be decisive in selecting a certain topology. Secondly, once a topology has been selected, one needs to determine the specifications of the building blocks. This can, of course, only be done when the impact of their nonidealities is known. A third reason involves the fact that it is computationally not interesting to perform high-level simulations at the circuit level.

To model the nonidealities at a high level, one can use two different strategies. One way is to derive analytical expressions identifying the SNR loss for each nonideality. Another approach is to use transfer function equations (e.g. in the z-domain) to fully simulate the behavior at a high level. The advantage of the first method clearly lies in the fact that it is computationally extremely efficient. However, it is not always straightforward to derive generally valid analytical expressions. They are only valid under certain conditions or pre-assumptions and merely form an approximation in a certain region. Complete high-level simulations on the contrary are more accurate (considering the high level) but seem to be computationally inattractive. However, considering the increasing computing power this is not completely the case. In a mathematical package like MATLAB there may be some speed penalty, but when the simulations are done in a real programming language like C we have found that the full simulation is fast enough, even for putting them within an optimization loop. Consequently, we will follow in this report the second approach only.

In the following chapter we will make a broad classification of the different nonidealities that have an impact on the system-level performance of  $\Delta\Sigma$  modulators. Based on this classification the subsequent chapters describe in more detail the error mechanisms affecting the modulator performance in each category.

## 2. Classification of the nonidealities

One can, of course, consider different classifications of the nonidealities of the building blocks. Most nonidealities occur with all topologies (single-loop, cascade, multi-bit) except the nonlinearity of the DAC in the feedback path which is of course only important for multi-bit structures. Note that this doesn't mean that the impact of these nonidealities is the same for all topologies. The DAC nonlinearity will be discussed separately in chapter 6.

All other nonidealities can be categorized in three broad classes, depending on the building block on which they have (the largest) impact. This leads to the integrator related nonidealities (chapter 3),

the comparator related ones (chapter 4) and other (shared between the building blocks or not) nonidealities (chapter 5). Both the integrator and the comparator are the major building blocks of a  $\Sigma\Delta$  modulator. A list of the considered nonidealities is given in Table 1. Another classification could be dependent on the type of error induced by the nonideality (noise increase, harmonic distortion, ...). We will consider switched-capacitor implementations only.

**Table 1: List of the considered nonidealities.**

<b>Class</b>	<b>Type</b>
<b>Integrator</b>	Finite operational amplifier gain Finite operational amplifier GBW Non-zero switch resistance Amplifier finite output swing Amplifier slew rate limitation Amplifier gain nonlinearity Nonlinear switch resistance Capacitor mismatch Capacitor nonlinearity
<b>Comparator</b>	Comparator offset Comparator hysteresis
<b>Other</b>	Clock jitter
<b>DAC</b>	DAC nonlinearity

### 3. Integrator related nonidealities

The integrator is the most important building block, especially when nonidealities are considered. Therefore it is imperative to know the alteration of its ideal transfer function in the presence of nonidealities. Of course, we should first define an ideal integrator. An ideal integrator (figure 3.1) can be described by the following transfer function in the z-domain (a 1-clock cycle delay is considered):

$$I(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{3.1}$$

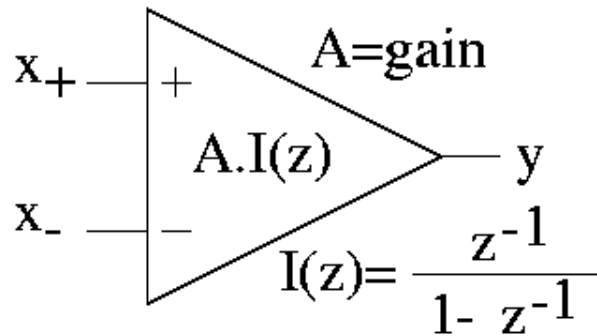


Figure 3.1: Ideal representation of an integrator.

Most generally, the different physical causes of linear degradation change this ideal integrator transfer function in three possible ways. Firstly, they can cause a gain error  $\alpha$  (smaller than 1) that is multiplied in the numerator of  $I(z)$ . Secondly, they can cause a pole error  $\beta$  (smaller than 1). Ideally the pole is located at  $z$  equal to 1 (see equation (3.1)). Both these changes in the integrator transfer function (shown in equation (3.2)) will eventually introduce low frequency quantization noise leakage.

$$I(z) = \frac{\alpha z^{-1}}{1 - \beta z^{-1}} \tag{3.2}$$

Thirdly, some nonidealities can also introduce an extra pole in the transfer function of the integrators. The resulting transfer function is then given by:

$$I(z) = \frac{\alpha z^{-1}}{1 - \beta z^{-1} + \gamma z^{-2}} \tag{3.3}$$

In [1] the effect of the gain and pole error have been analysed. We will limit ourselves in this report to summarising the effect of different nonidealities on the gain and pole error. Once these dependencies are known, equations (3.2) or (3.3) can be used in a behavioral-level simulator.

We will not take the influence of OTA parasitic and load capacitance into account because these parameters are undetermined at the system level. It is, however, possible to verify the resulting small deviation after the building blocks have been designed.

### 3.1. Finite operational amplifier gain

Figure 3.2 presents a model for a switched-capacitor integrator during both the sampling and the integration phases. In this model the amplifier is simply represented by a voltage-controlled voltage source with finite gain A and no other effects are considered.

The transfer function of this integrator structure is given by [1], [4], [5]:

$$I(z) = \frac{C_S}{C_I} \frac{\rho_2 z^{-1}}{1 - \frac{\rho_2}{\rho_1} z^{-1}} \quad (3.4)$$

where  $\rho_1$  and  $\rho_2$  are the closed-loop static errors:

$$\rho_1 = \frac{Af_{dc1}}{1 + Af_{dc1}} \quad (3.5)$$

$$\rho_2 = \frac{Af_{dc2}}{1 + Af_{dc2}} \quad (3.6)$$

and  $f_{dc1}$  and  $f_{dc2}$  are the DC feedback factors during the sampling and integration phase respectively:

$$f_{dc1} = 1 \quad (3.7)$$

$$f_{dc2} = \frac{C_I}{C_S + C_I} \quad (3.8)$$

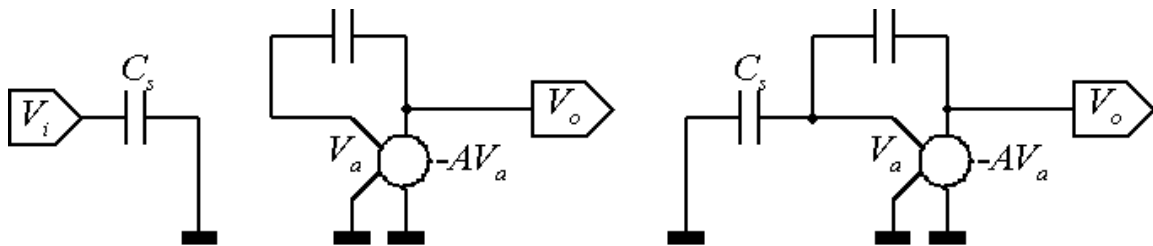


Figure 3.2: SC integrator with finite gain amplifier (left: sampling phase, right: integration phase).

### 3.2. Finite operational amplifier GBW

In the previous section it was assumed that the operational amplifier instantaneously settles to its final value. A real integrator, however, has some limitations in frequency due to poles that limit the speed of the settling process. Here we will consider the effect of a finite closed-loop dominant pole on the transfer function of an integrator. In figure 3.3 the amplifier is modelled by an OTA with a finite output conductance  $g_o$  and a transconductance  $g_m$ .

The transfer function of this integrator can be calculated yielding [1], [4], [5], [6]:

$$I(z) = \frac{C_S}{C_I} \frac{\rho_2(1-\delta_2)z^{-1}}{1 - \frac{\rho_2}{\rho_1}(1-\delta_2(1-\frac{\rho_1}{\rho_2}))z^{-1}} \quad (3.9)$$

where  $\rho_1$  and  $\rho_2$  are still given by (3.5) and (3.6) respectively. The amplifier gain used in these equations is:

$$A = \frac{g_m}{g_o} \quad (3.10)$$

The parameter  $\delta_2$  represents the settling error in the integration phase. It is expressed by:

$$\delta_2 = \exp\left(-\frac{g_m}{C_S} \frac{\tau_2}{\rho_2}\right) \quad (3.11)$$

where  $\tau_2$  represents the time available for settling during the integration phase.

This shows that the transconductance of the amplifier combined with the sampling capacitor create a closed loop pole that limits the speed of the settling process.

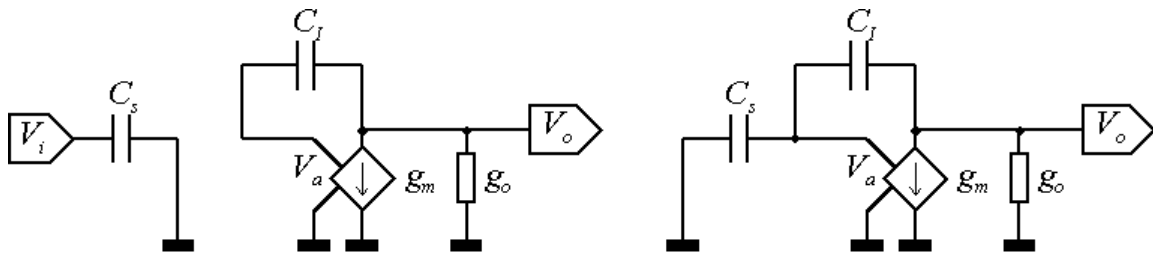


Figure 3.3: SC integrator with finite gain and finite bandwidth amplifier (left: sampling phase, right: integration phase).

### 3.3. Non-zero switch resistance

While in the previous sections only effects related to the used amplifier were considered, an integrator also contains switches. Until now a zero switch resistance in the "on" phase was assumed, implying that the charge transfer from the sampling capacitor to the integration capacitor is instantaneous. In an actual implementation the on-resistance of the switches cannot be neglected and gives, in combination with the sampling capacitor, rise to an RC time constant.

We will now consider two cases depending on the model of the amplifier (section 3.1 or 3.2).

#### 3.3.1. Instantaneous OTA settling

This case is illustrated in figure 3.4 and yields the following expressions:

$$I(z) = \frac{C_S}{C_I} \frac{\rho_2(1-\delta_1)(1-\delta_2)z^{-1}}{1-\beta z^{-1} + \gamma z^{-2}} \quad (3.12)$$

with the following parameter definitions:

$$\beta = \frac{\rho_2}{\rho_1} + (\delta_1 + \delta_2)\left(1 - \frac{\rho_2}{\rho_1}\right) + \delta_1\delta_2 \frac{\rho_2}{\rho_1}$$

$$(3.13)$$

$$\gamma = \delta_1\delta_2 \quad (3.14)$$

where the settling errors during the sampling and integration phase are respectively:

$$\delta_1 = \exp\left(-\frac{\tau_1}{RC_S}\right) \quad (3.15)$$

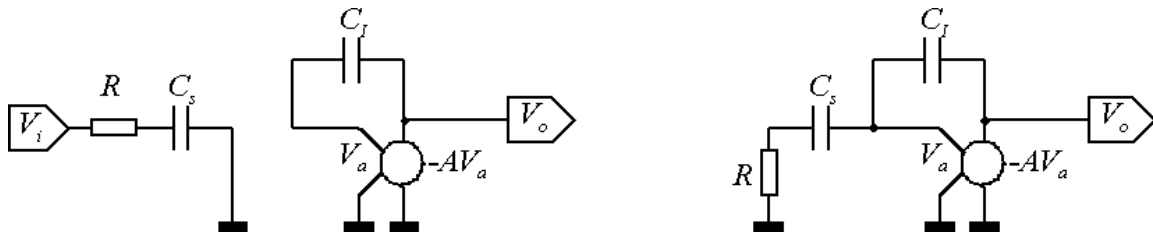


Figure 3.4: SC integrator considering non-zero switch resistance (left: sampling phase, right: integration phase) - amplifier with finite gain.

$$\delta_2 = \exp\left(-\frac{\rho_1}{\rho_2} \frac{\tau_2}{RC_S}\right) \quad (3.16)$$

The expressions for the factors  $\rho_1$  and  $\rho_2$  are still given by (3.5) and (3.6).

Note that the transfer function of the integrator (equation (3.12)) now exhibits two poles: one very close to unity that can be directly related to a pole error in the integrator transfer function, and one very close to zero that increases the gain error of the integrator. This is according to equation (3.3).

### 3.3.2. Frequency limited OTA

If we take the frequency limitations of the amplifier into account, the model becomes as shown in figure 3.5. The transfer function now becomes somewhat more involved. It is still given by equation (3.12) but now with the following parameter definitions:

$$\beta = \frac{\rho_2}{\rho_1} + \delta_1 \lambda_2 + \delta_2 \left(1 - \frac{\rho_2 / \rho_1}{1 + \lambda_1} - \frac{\lambda_1}{1 + \lambda_1} (f_{dc2} + \rho_2 (1 - f_{dc2}))\right) \quad (3.17)$$

$$\gamma = \frac{\delta_1 \delta_2}{1 + \lambda_1} \left(\lambda_2 + \left(\frac{\rho_2}{\rho_1} + \lambda_2\right) \left(\frac{\rho_2}{\rho_1} + \rho_1 \lambda_1 \left(\frac{\rho_2}{\rho_1} + \lambda_2\right)\right)\right) \quad (3.18)$$

where the settling errors are now given by:

$$\delta_1 = \exp\left(-\frac{\tau_1}{RC_S}\right) \quad (3.19)$$

$$\delta_2 = \exp\left(-\frac{g_m}{C_S} \frac{\tau_2}{\rho_2 (1 + \lambda_1)}\right) \quad (3.20)$$

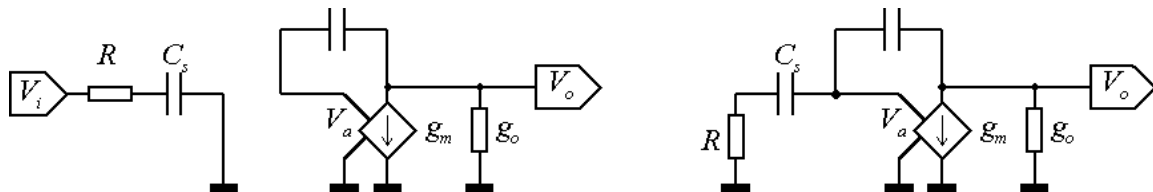


Figure 3.5: SC integrator considering non-zero switch resistance (left: sampling phase, right: integration phase) - amplifier with finite gain and finite GBW.

with the following auxiliary parameters:

$$\lambda_1 = g_m R / \rho_1 \quad (3.21)$$

$$\lambda_2 = (1 - f_{dc})(1 - \rho_2) \quad (3.22)$$

### 3.4. Amplifier finite output swing

The output voltage of a real amplifier is not rail-to-rail but bounded to a voltage smaller than the supply voltage (determined by the drain-source saturation voltages of the output transistors). This effect is easy to take into account at a high level by clipping the output voltage (see equation (3.23)) if it exceeds a certain value  $V_{osw}$  (output swing):

$$\text{if } |V_o| > V_{osw} \text{ then } V_o = V_{osw} * \text{sgn}(V_o) \quad (3.23)$$

### 3.5. Amplifier slew rate limitation

In the previous sections it was assumed that the amplifier always remains in its linear region of operation. This is a valid assumption during the sampling phase, since the integration of the previous input voltage is almost completely settled and so the amplifier input node barely varies during this phase. But during the integration phase, the sampling capacitor is simply connected to the input of the amplifier. A large sampled value can then drive the amplifier out of its linear region of operation, and the amplifier can start to slew.

In [1] the effect of amplifier slew rate is analyzed following the approach in [7]. Basically, when the sampling phase has finished, there are two possibilities; either the amplifier starts the integration phase in its linear region or it starts the integration phase slewing and enters its linear region before the end of the integration phase. This is illustrated by the following equations:

$$|v_i| \leq \frac{I_M}{g_m f_{ff}} \quad (3.24)$$

$$|v_i| > \frac{I_M}{g_m f_{ff}} \quad (3.25)$$

In these equations  $v_i$  represents the sampled input signal,  $I_M$  the maximum output current of the amplifier,  $g_m$  its transconductance and  $f_{ff}$  the feedforward factor for the sampled input voltage:

$$f_{ff} = \frac{C_S(C_I + C_L)}{(C_S + C_P)C_P + (C_S + C_P + C_I)C_L} \quad (3.26)$$

where  $C_S$  and  $C_I$  are the sampling and integration capacitors and  $C_P$  and  $C_L$  are the amplifier parasitic input capacitance and equivalent capacitive load at the output of the integrator respectively.

A complete derivation of the output voltages in the cases expressed by (3.24) and (3.25) can be found in [1]. Note that the equations derived in [1] are for a zero switch 'on' resistance. The resulting output voltage for the case of linear settling is given by:

$$v_o[n] = \varepsilon_2 f_{ff} \frac{g_m^2}{g_{m1}g_{m2}} \left( 1 + \frac{g_o}{g_m f_{dc2}} \left( \frac{1 - \varepsilon_1}{f_{dc1}} - \frac{1}{f_{dc2}} - \frac{g_o}{g_m} \frac{\varepsilon_1}{f_{dc1}f_{dc2}} \right) \right) v_i[n-1] + \frac{g_m^2}{g_{m1}g_{m2}} \left( 1 + \frac{g_o}{g_m f_{dc1}} (1 - \varepsilon_2) + \varepsilon_2 \frac{g_o}{g_m f_{dc2}} + \varepsilon_2 \varepsilon_1 \frac{g_o}{g_m f_{dc1}} \left( 1 + \frac{g_o}{g_m f_{dc2}} \right) \right) \left( v_o[n-1] + \frac{C_S}{C_I} v_i[n-1] \right) \quad (3.27)$$

and for nonlinear settling by:

$$v_o[n] = \varepsilon_2 \frac{g_m}{g_{m1}g_{m2}} \left( 1 + \frac{g_o}{g_m f_{dc2}} \left( \frac{1 - \varepsilon_1}{f_{dc1}} - \frac{1}{f_{dc2}} - \frac{g_o}{g_m} \frac{\varepsilon_1}{f_{dc1}f_{dc2}} \right) \right) I_M \text{sign}(v_i[n-1]) + \frac{g_m^2}{g_{m1}g_{m2}} \left( 1 + \frac{g_o}{g_m f_{dc1}} (1 - \varepsilon_2) + \varepsilon_2 \frac{g_o}{g_m f_{dc2}} + \varepsilon_2 \varepsilon_1 \frac{g_o}{g_m f_{dc1}} \left( 1 + \frac{g_o}{g_m f_{dc2}} \right) \right) \left( v_o[n-1] + \frac{C_S}{C_I} v_i[n-1] \right) \quad (3.28)$$

In these equations a number of parameter definitions have been introduced as follows:

$$f_{dc1} = \frac{C_I}{C_P + C_I} \quad (3.29)$$

$$f_{dc2} = \frac{C_I}{C_S + C_P + C_I} \quad (3.30)$$

$$g_{m1} = g_m + g_o / f_{dc1} \quad (3.31)$$

$$g_{m2} = g_m + g_o / f_{dc2} \quad (3.32)$$

$$\varepsilon_1 = e^{-\frac{g_{m1}t}{C_{eq1}}} \quad (3.33)$$

$$\varepsilon_2 = e^{-\frac{g_{m2}t}{C_{eq2}}} \quad (\text{linear settling}) \quad (3.34a)$$

$$\varepsilon_2 = e^{-\frac{g_m^2(t-t_s)}{C_{eq2}}} \quad (\text{nonlinear settling}) \quad (3.34b)$$

$$C_{eq1} = C_P + C_L(C_P + C_I)/C_I \quad (3.35)$$

$$C_{eq2} = (C_S + C_P) + C_L(C_S + C_P + C_I)/C_I \quad (3.36)$$

$$t_s = f_{ff} \frac{C_{eq2}}{I_M} \left( |v_i| - \frac{I_M}{g_m f_{ff}} \right) \quad (3.37)$$

### 3.6. Amplifier gain nonlinearity

In section 3.1 we considered the case of finite amplifier gain. In reality, the gain is not only finite but also dependent on the output voltage. Assuming that the gain nonlinearity can be expressed by a Taylor series of second order, we get:

$$A(v_0) = A_0(1 + av_0 + bv_0^2) \quad (3.38)$$

where a and b are the linear and quadratic voltage coefficients of the gain. Due to the output voltage dependency, this problem needs to be solved iteratively.

### 3.7. Nonlinear switch resistance

In section 3.3 the effect of a non-zero switch on-resistance was mentioned. In practice, this resistance is also dependent on the voltage across it. In [1] some equations are derived for (almost) constant input signals. For sinusoidal input signals one should resort to numerical solutions. The result is harmonic distortion.

### 3.8. Capacitor mismatch

The integrator transfer function of equation (3.2) is multiplied by the gain defined by the ratio of the sampling and the integration capacitor ( $C_S/C_I$ ) in a switched-capacitor implementation (see figure 3.1). A mismatch of the capacitor values resulting in an error of the integrator gain can be modeled

by adjusting their ratio at the high level. Note that a capacitance ratio has a much higher precision than the absolute value of the respective capacitors. As a result, this effect is normally not a problem for single-loop topologies. But the requirement for cascade structures is more strict due to the effect of incomplete noise cancellation.

### 3.9. Capacitor nonlinearity

The capacitor value is in reality dependent on the voltage stored on it. Again, we approximate this by a second-order Taylor series:

$$C(v) = C_0(1 + av + bv^2) \quad (3.39)$$

As a result of this dependency, the output voltage of the integrator has to be found iteratively.

## 4. Comparator related nonidealities

Ideally, a comparator can be described by:

$$V_{in} \leq V_{ref} \quad V_{out} = V_{out-} \quad (4.1)$$

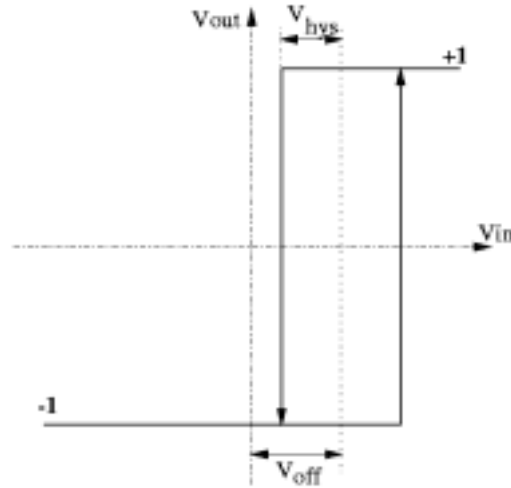
$$V_{in} > V_{ref} \quad V_{out} = V_{out+} \quad (4.2)$$

Where  $V_{in}$  and  $V_{out}$  are the input and output voltages of the comparator,  $V_{ref}$  is the reference voltage for the comparison and  $V_{out+}$  and  $V_{out-}$  are the positive and negative values of the output respectively (mostly the digital supply voltages).

Two of the most important specifications for a comparator used in a  $\Delta\Sigma$  modulator are offset and hysteresis as illustrated in figure 4.1. These are discussed next.

### 4.1. Comparator offset

Since the description of an ideal comparator at a high level is just a comparison between two values, one can easily add the comparator offset to the reference value. This simple alteration suffices to use it at a behavioral level. Equations (4.1) and (4.2) now become:



**Figure 4.1: Comparator transfer function illustrating offset and hysteresis.**

$$V_{in} \leq (V_{ref} + V_{off}) \quad V_{out} = V_{out-} \quad (4.3)$$

$$V_{in} > (V_{ref} + V_{off}) \quad V_{out} = V_{out+} \quad (4.4)$$

#### 4.2. Comparator hysteresis

Instead of comparing the input with one reference voltage one can use two reference voltages (plus or minus the hysteresis value) depending on the previous output value. This requires a memory function. Again, this is trivial at a behavioral level. Equations (4.1) and (4.2) now depend on the previous output value ( $V_{out\_prev}$ ):

CASE 1 -  $V_{out\_prev} = V_{out-}$ :

$$V_{in} \leq (V_{ref} + V_{hys}) \quad V_{out} = V_{out-} \quad (4.5)$$

$$V_{in} > (V_{ref} + V_{hys}) \quad V_{out} = V_{out+} \quad (4.6)$$

CASE 2 -  $V_{out\_prev} = V_{out+}$ :

$$V_{in} \leq (V_{ref} - V_{hys}) \quad V_{out} = V_{out-} \quad (4.7)$$

$$V_{in} > (V_{ref} - V_{hys}) \quad V_{out} = V_{out+} \quad (4.8)$$

### 4.3. Comparator offset and hysteresis combined

Finally, combining offset and hysteresis yields the following equations:

$$V_{in} \leq (V_{ref} + V_{off} - \text{sgn}(V_{out\_prev}) * V_{hys}) \quad V_{out} = V_{out-} \quad (4.9)$$

$$V_{in} > (V_{ref} + V_{off} - \text{sgn}(V_{out\_prev}) * V_{hys}) \quad V_{out} = V_{out+} \quad (4.10)$$

## 5. Other nonidealities

We will discuss only clock jitter here.

### 5.1. Clock jitter

In a SC implementation, clock jitter causes random imprecisions on the actual sampling instant (non uniform sampling). Although clock jitter is also present in the integration phase, it can be neglected because of the following reason. The charge transfer during the integration phase, from the sampling to the integration capacitor, has to be quite accurate, otherwise significant performance degradation results. Actually, the settling error during the integration phase has to be very small, almost of the order of the required resolution. Consequently, a timing uncertainty during the integration phase originates an error in the integrated value equal to the difference between two settling errors: one considered at the actual sampling instant and the other considered at the ideal sampling instant (without clock jitter). This error is for all practical purposes very small and can be ignored.

For the sampling phase, on the other hand, consider a sinusoidal signal with amplitude  $A$  and frequency  $f_i$ :

$$v_i(t) = A \sin(2\pi f_i t) \quad (5.1)$$

Consider that the clock jitter is described by a Gaussian random variable  $\Delta T$  with an average value of zero and a standard deviation  $\sigma_{\Delta T}$ . Due to the clock jitter, the sampled value of the input signal has an inaccuracy given by:

$$\Delta V = v_i(nT + \Delta T) - v_i(nT) \approx 2\pi f_i A \cos(2\pi f_i nT) \Delta T \quad (5.2)$$

in which T is the sampling period and n the sampling index. This inaccuracy is then a Gaussian random process with a variance given by [8]:

$$\sigma_{\Delta v}^2 = \frac{(2\pi f_i A)^2}{2} \sigma_{\Delta T}^2 \quad (5.3)$$

In the frequency domain this random error has a uniform frequency distribution. Because of the oversampled nature of  $\Sigma\Delta$  converters only 1/OSR (oversampling ratio) of the total clock jitter noise falls in the signal band. Therefore, the in-band noise power  $N_j$  caused by clock jitter is given by:

$$N_j = \frac{(2\pi f_i A)^2 \sigma_{\Delta T}^2}{2 \text{OSR}} \leq \frac{(\pi f_s A)^2 \sigma_{\Delta T}^2}{2 \text{OSR}^3} \quad (f_{i,\max} = \frac{f_s}{2\text{OSR}}) \quad (5.4)$$

The ratio between the input signal power and the noise power caused by clock jitter is then:

$$\text{SNR}_j = \frac{\text{OSR}^3}{(\pi f_s \sigma_{\Delta T})^2} \quad (5.5)$$

Based on equation (5.1) a behavioral model could look like this:

$$v_i(t) = A \sin(2\pi f_i (t + \sigma'_{\Delta T} \frac{1}{f_s})) \quad (5.6)$$

Where  $\sigma'_{\Delta T}$  is the standard deviation of the clock jitter relative to the clock period.

## 6. DAC nonlinearity

Despite the improvement in performance and in stability [3], the main problem of multi-bit  $\Sigma\Delta$  converters is the linearity of the DAC in the feedback path. In order not to degrade the system performance, the linearity of the DAC should be as good as the overall wanted resolution of the converter. In [3] different solutions to this problem are surveyed. In [9] offset, gain and nonlinearity are discussed. The nonlinearity is the most important error in practical cases [9]. Because the INL of

the transfer curve does not fully specify the converter nonlinearity, in [9] it is supposed that the converter presents a third-order nonlinearity.

At the behavioral level, the quantizer that consists of a simple comparator for the single bit case, has to be replaced by several comparators (dependent on the number of levels or bits). The nonlinearity of the DAC can then be modeled by taking a number (proportional to the output value) of unity elements (as in a real implementation), but then with a random distribution around each unity element. The  $n$ th output sample of the  $i$ th integrator is given by equation (6.1) for the ideal case, where  $a$  represents the integrator gain coefficient and  $y$  the quantizer output.

$$v(n, i) = v(n-1, i) + a(i) * (v(n-1, i-1) - y(n-1)) \quad (6.1)$$

Instead of using the quantizer output directly, one can use the sum of as many (say  $k$ ) unity elements ( $u$ ) according to the quantizer output  $y$ . This is illustrated by the following equations:

$$v(n, i) = v(n-1, i) + a(i) * (v(n-1, i-1) - v_{fb}) \quad (6.2)$$

$$v_{fb} = \frac{u_i}{k} \quad (6.3)$$

$$v_{fb} = \frac{v_{fb} - 2^{B-1}}{2^{B-1}} \quad (6.4)$$

The last equation normalizes the DAC voltage, with  $B$  the number of bits.

The DAC nonlinearity is then modeled by changing the unity elements according to a random distribution. So, in the case of the unity element vector  $u$ :

$$u = u * NORM(1, \sigma, 2^B) \quad (6.5)$$

where  $NORM$  represents a normal distribution with mean value  $1$ , variance  $\sigma$  and length  $2^B$ .

## 7. Conclusions

An overview of  $\Delta\Sigma$  modulator nonidealities was given in this report. The major error mechanisms have been discussed together with a way to model them at a high level during system-level

optimization. This allows to derive building block specifications for all components constrained by a set of system specifications at a high level. It also allows to trade off different topologies given a set of specifications.

## References

- [1] A. Marques, "High Speed CMOS Data Converters", Ph.D. thesis K.U. Leuven , January 1999.
- [2] F. Op 'T Eynde, W. Sansen, "Analog Interfaces for Digital Signal Processing Systems", Kluwer Academic Publishers, ISBN 0-7923-9348-1, June 1993.
- [3] Y. Geerts, M. Steyaert, "Deliverable D2.1.1: Guidelines for implementation of CMOS multibit oversampling modulators", 1999.
- [4] K. Martin and A. Sedra, " Effects of the Op Amp Finite Gain and Bandwidth on the Performance of Switched-Capacitor Filters", IEEE Transactions on Circuits and Systems, vol. 28, no. 8, August 1981, pp. 822-829.
- [5] G. Temes, " Finite Amplifier Gain and Bandwidth Effects in Switched-Capacitor Filters", IEEE Journal of Solid-State Circuits, vol. 15, no. 3, June 1980, pp. 358-361.
- [6] G. Fischer and G. Moschytz, "On the Frequency Limitations of Switched Capacitor Filters", IEEE Journal of Solid-State Circuits, vol. 19, no.4, August 1984, pp. 510-518.
- [7] W. Sansen, H. Quieting and K. Halonen, "Transient Analysis of Charge Transfer in SC Filters - Gain Error and Distortion", IEEE Journal of Solid-State Circuits, vol. 22, no.2, April 1987, pp. 268-276.
- [8] B. Boser and B. Wooley, "The design of sigma-delta modulation analog-to-digital converters", IEEE Journal of Solid-State Circuits, vol. 23, no.6, December 1988, pp. 1298-1308.
- [9] F. Medeiro, B. Perez-Verdú and A. Rodríguez-Vázquez, "Top-Down design of High-Performance Sigma-Delta Modulators", Kluwer Academic Publishers, ISBN 0-7923-8352-4, November 1998.