

SOI Hall plate characterization

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I. INTRODUCTION

This work is part of the TERMIS project for an integrated Hall sensor able to operate from $-55\text{ }^\circ\text{C}$ to temperatures exceeding $300\text{ }^\circ\text{C}$. This paper covers the design of the Hall plate alone.

Definition and basic equations of Hall effect for resistive sensors are only summarized here, since a complete reference about theory of Hall sensors can be found in [4]. Alternative sensors made of magneto-mos structures are also briefly discussed. Measurements of the resistive plate are presented. The case of spinning-current offset cancellation is discussed as well. Finally, an electrical circuit suitable for Spice simulations is proposed.

II. DEFINITIONS

It is assumed that the magnetic field is low enough to consider mobility constant. When the sensor is biased by a current I_b , the Hall voltage V_H equals [4, eqn (4.48)]:

$$V_H = GI_b \frac{r_H}{qnt_{si}} B_{\perp} \quad (1)$$

Eq. 1 can be rewritten with $S_I = G \frac{r_H}{qnt_{si}}$ as

$$V_H = S_I I_b B_{\perp} \quad (2)$$

In first a approximation, the sensor sensitivity S_I does not change with temperature: it is not dependent on mobility and majority concentration n is assumed to remain constant. S_I however depends on the *Hall factor* r_H , which is the ratio between drift mobility μ and Hall mobility¹ μ_H . This factor, close to unity, tends to increase with the temperature and must be compensated. [4] also provides equations when the device is biased with a voltage, but it was preferred in this work to think of the sensor as a resistor and compute its bias current with its conductance g_0 . Moreover, the conductance is decomposed into a factor which depends on the geometry of the sensor, the normalized conductance g_n , and the actual sheet conductivity of the material:

$$g_0 = g_n q \mu n t_{si} \quad (3)$$

III. IMPLEMENTATION

Besides classical four contacts resistive sensors, several other types of devices are able to sense magnetic fields, like resistors, diodes or transistors. For instance, a split drain magneto-mos device has been investigated as an alternative: a MOS transistor is drawn with two separated drains, as shown on figure 1. Any magnetic field causes a deviation of the carriers in the transistors, which in turn causes an imbalance in the drain currents.

¹Mobilities associated with fields due to the electrical bias (μ) and due to the Hall effect (μ_H) are different.

TABLE I
DEFINITIONS

Parameter	Relation
Elementary charge	q
MajorityCarrier concentration	n
Conduction mobility	μ
Magnetic induction	B
Sensor layer thickness	t_{si}
Hall voltage for inf. small contact	$V_{H\infty}$
Correction for actual contact	$G = \frac{V_H}{V_{H\infty}}$
Conductivity at $B = 0$	$\sigma = q\mu n$
Isotropic Hall scattering factor	r_{H0}
Anisotropic factor	$a = 0.87$
Hall factor	$r_H = ar_{H0}$
Hall mobility	$\mu_H = -r_H\mu$
Hall absolute voltage	$V_H = G \frac{r_H}{qnt_{si}} I_b B_{\perp}$
Normalized sensor conductance	$g_n = \frac{R_{sh}}{R}$
Sensitivity	$S_I = G \frac{r_H}{qnt_{si}}$

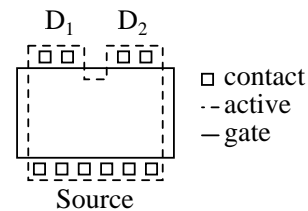


Fig. 1. Split drain magneto-mos layout.

Measurements showed sensitivity and offsets figures comparable to a resistive Hall sensor, with typical offsets about 30 mT. The offsets are strongly dependent on the MOS voltage biases as well as on the temperature. As a consequence, this solution is not applicable, because there is no robust methods to reduce the sensor offsets when the temperature changes. On the other hand, spinning-current method [1] applied to resistive sensors allows a continuous reduction of offsets with temperature and aging.

A. Actual sensor

A.1 Shape optimization

Spinning current offset cancellation technique requires a structure which is invariant by rotation of 90° . Within this constraint, the shape is a compromise between the resulting resistance of the shape, hence sensor conductance g_n which limits the maximum bias current, and short-circuit effect of contacts, hence the geometry correction factor G . We followed recommendation in [2][3] and shaped the sensor like a Greek cross,

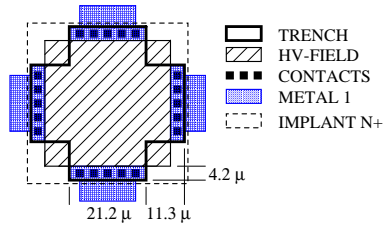


Fig. 2. Layout of the actual sensor.

illustrated at figure 2.

A.2 Layer optimization

In order to get the highest sensitivity for a given voltage bias, or a given voltage supply in the case of a current biased sensor, it is desirable to have a material with the highest mobility, which means a lowly doped N layer. At first, N-well ($N_D = 3.98 \cdot 10^{16} / \text{cm}^3$) layer was tried. The sensor was formed with a MOS structure: polysilicon gate, thin oxide, N-well, buried oxide and substrate. The polysilicon gate is needed in order to obtain the N-well doping. Such a sensor has however an important drawback. The lowly doped N-well does not behave as a linear resistor. Depending on the difference between the silicon film potential and the polysilicon gate potential, the silicon layer can be in inversion, in depletion or in accumulation. Since the sensor is ideally biased with the maximum supply, 5 V, and the polysilicon gate potential is normally between 0 V and 5 V, it is not possible to ensure a constant accumulation level over the whole sensor layer. As a result, the relation between the bias current in the sensor and the sensitivity is not linear any longer.

Therefore, N-drift layer ($N_D = 6.08 \cdot 10^{16} / \text{cm}^3$), which is more doped, was preferred. Figure 2 show the actual layout. N-drift layer is selected with HV-field oxide and N+ implantation. Compared with N-well, this solution does not suffer from the coupling with a gate at a constant potential.

IV. SENSOR CHARACTERISTICS

A. Resistivity

The resistance of the N-drift Hall cross was measured (figure 3). The N-drift resistance linearity is better than 1.5%/V. Figure 6 illustrates polynomial fits of the relative resistivity of the plate for two different voltage biases. The resistivity almost triples between room temperature and 300 °C.

B. Magnetic sensitivity

The normalized sensitivity S_I of the N-drift sensor was measured around 205 V/AT at room temperature (fig. 7). This value is very good for CMOS sensors, and a bias current I_b of 300 μA yields a sensor gain S of 62 mV/T.

C. Offset

The Hall plate offset has been measured as a function of temperature, fig. 8 shows the result for a typical sample. On other samples, offsets increase continuously with the temperature. The expected offset correction obtained from spinning current or spatial correlation between several sensors has been measured as well. Two measurements are performed for each

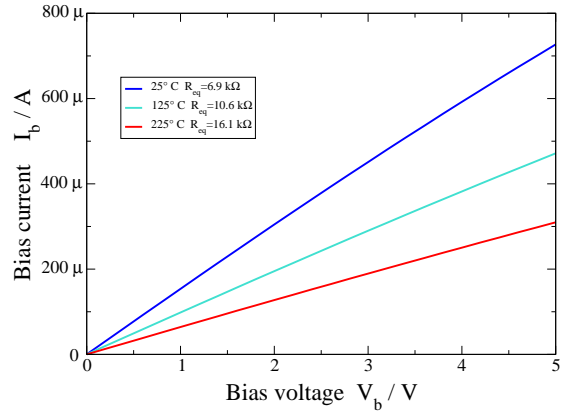


Fig. 3. N-drift Hall cross I/V measurements.

TABLE II
RESULTS

Parameter	Symb.	Unit	300 ° K	425 ° K	525 ° K
Measured conduct.	g_0	μS	146	94	62
Normalized sens.	S_I	V/AT	205	216	226
Offset without corr.	B_{Oi}	mT	35	33	64
Offset with corr.	B_{Oc}	mT	3.8	1.0	0.6

sensor: current bias from A to C, and from B to D, which result in two Hall voltages V_{H1} and V_{H2} (see figure 4). Ideally, the average of these two measurement should be free of the sensor offset. Offset figures reported in table II. Later measurement on sensors integrated with a modulator and an amplifier, packaged in ceramic, actually showed lower residual offsets (max. 1.5 mT) than reported here. We suspect that time separating the measurement of V_{H1} and V_{H2} is too long.

Spatial correlation between different sensors closely located has been measured as well, but the results showed it is not possible to expect significant offsets reduction by cross coupling several sensors.

D. Low frequency noise

Low frequency noise ($1/F$) has been measured at room temperature, figure 9. Noise power spectrum density was found to be more than 30dB higher than conventional CMOS sensors [2]. Beside the smaller area of this sensor, we suspect that the buried oxide interface contributes to the noise increase: it has been reported literature that SOI MOS devices exhibit increased $1/F$ noise compared to classical “bulk”. It is however been demonstrated that spinning current modulation of the sensor significantly reduces the noise at low frequency.

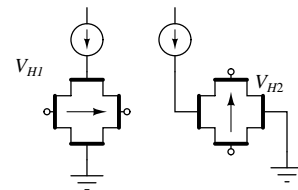


Fig. 4. Offset compensation principle.

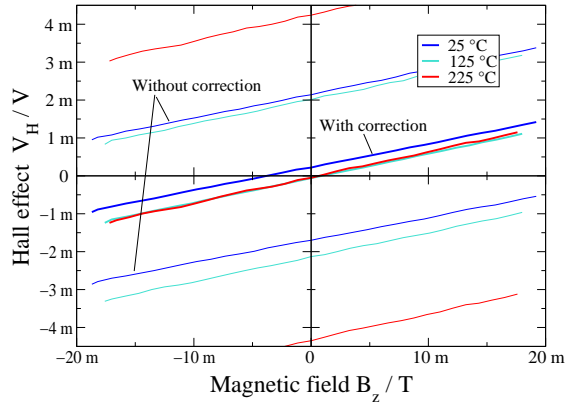


Fig. 5. Sensitivity and offsets measurements at 25, 125 and 225 °C. *With correction* stands for the average of V_{H1} and V_{H2} measurements (see figure 4).

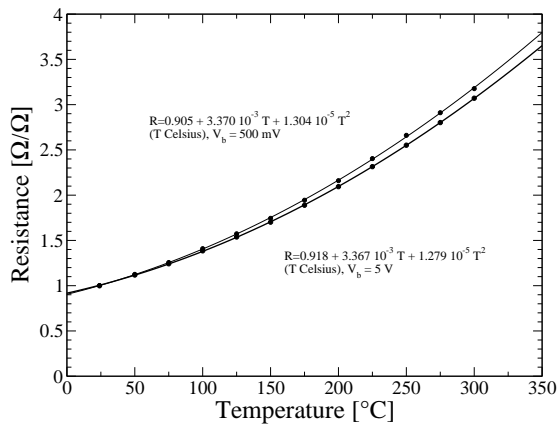


Fig. 6. Measured of the typical relative resistivity of N-drift (normalized against 25 °C value) and fitted coefficients for a bias of 5 V and 500 mV.

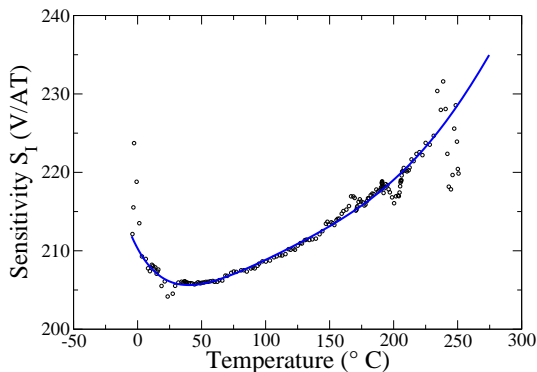


Fig. 7. Normalized magnetic sensitivity of the Hall plate. (Bias at 3.2 V)

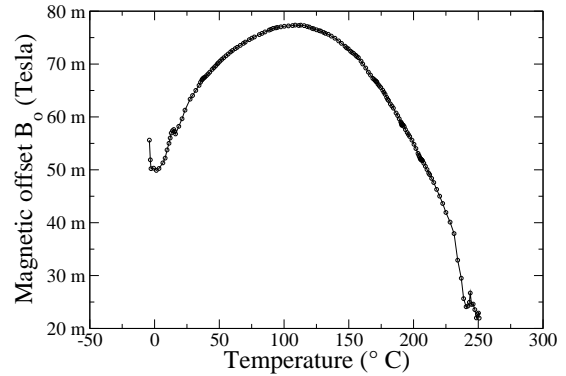


Fig. 8. Measured magnetic offset of a Hal plate sample without correction. (Bias at 3.2 V, Ceramic DIL16 package).

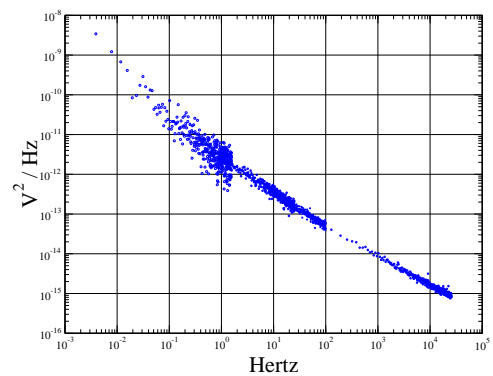


Fig. 9. Low frequency noise power spectral density at room temperature, with a voltage bias of 3V. Curve fit is $y = 2 \cdot 10^{-12} \cdot x^{-0.78}$

V. SIMULATION MODEL

Several electrical circuits have been proposed in order to simulate Hall sensors with SPICE. We suggest yet another circuit, figure 10, which models correctly currents flowing from opposite nodes, for example A to C, as well as current flowing between contiguous nodes, like from A to B. This point is important for transient simulation of spinning current. The current controlled voltage sources model the Hall effect in the layer. The SPICE sub circuit below works successfully with SmartSpice. On the other hand, PSpice needs slight modification because it requests a different syntax for `.PARAM` statements as well as a different syntax for A elements. This model is calibrated by two measurements of currents flowing between nodes A-B and A-C.

$$V_{ha} = \frac{S_I}{2} I_b B_{\perp} \quad (4)$$

```
* EPFL-LEG
* Sub circuit for Hall sensor
* for SmartSpice
.PARAM HC_RSH0=5000
.PARAM HC_rh=0.8
.PARAM HC_tsi=220e-9
.PARAM HC_g1=0.55
.PARAM HC_g2=0.52
.PARAM HC_G=0.67
.PARAM HC_N=6.1E22
.PARAM HC_RSH='HC_RSH*(0.918+3.367e-3*TEMP+1.297e-5*(TEMP*TEMP))'
.PARAM HC_r1='HC_RSH/HC_g1'
```

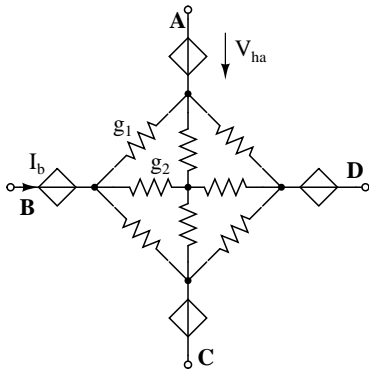


Fig. 10. Equivalent electrical circuit for the Hall sensor. The voltage source equation is given at (4).

```
.PARAM HC_r2='HC_RSH/HC_g2'
* Temp. dependence of HC_gain neglected!!!
.PARAM HC_gain='0.5*HC_G*HC_rh/(HC_N*HC_tsi*1.6E-19)'
* Nodes ABCD are the Hall plate 4 contacts
* Node F is the magnetic field (1V=1T)
* Node S is SOI backgate
.SUBCKT hallcross A B C D F S
C1 X S 100f
Rab A2 B2 HC_R1
Rbc B2 C2 HC_R1
Rcd C2 D2 HC_R1
Rda D2 A2 HC_R1
Rax A2 X HC_R2
Rbx B2 X HC_R2
Rcx C2 X HC_R2
Rdx D2 X HC_R2
A1a A A2 V=HC_gain*I(A1b)*V(F,0)
A1b B B2 V=HC_gain*I(A1c)*V(F,0)
A1c C C2 V=HC_gain*I(A1d)*V(F,0)
A1d D D2 V=HC_gain*I(A1a)*V(F,0)
.ENDS
```

VI. DISCUSSION

This SOI Hall plate shows a high sensitivity, which is very stable for temperature up to 300 °C. Thanks to the high sensitivity, low bias currents < 200 μ A can be used, allowing the design of low power sensors. If spinning current offsets cancellation is used, total offset, including integrated amplifiers and packaging, can be reduced to 1.5 mT, with at the same time excellent noise levels. These figures are comparable with other CMOS sensors, which are them self limited to 150 °C. Moreover, the Hall plate integrated with its electronics has shown that the modulation frequency, at room temperature, can exceed 1 MHz.

REFERENCES

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- [2] Hubert Blanchard. *Hall Sensors with Integrated Magnetic Flux Concentrators*. PhD thesis, École Polytechnique Fédérale de Lausanne, Switzerland, May 1999.
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- [4] R S Popović. *Hall effect devices*. Adam Hilger, 1991.