Workshop on A/D Converters for Telecommunication

# High-Bandwidth Low-Pass SD A/D Converters

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22nd October, 2001

# Outline

❑ Introduction

❑ Architectures for broad-band low-pass ΣΔ Modulators

- Quantizer
- Loop-filter

❑ Design example: A 50mW, 14bit 2.5MS/s ΣΔ Modulator

- Motivation
- Analog modulator
- Measurement results

❑ Conclusion

# Introduction

❑ ΣΔ converters suited for more than 13bit resolution.

❑ Broad-band ΣΔ converters here assumed to have >1MS/s and <10MS/s conversion rate

❑ High converter dynamic range in communication applications:

- Relaxed analog front-end requirements
- Simultaneous channel conversion (e.g. in the base station)
- Complex modulation methods with better bandwidth / data rate efficiency (OFDM)

# Architecture Considerations

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## Architectures for Broad-Band Low-Pass SD Modulators

# Architecture Trade-offs

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Unchanged SNR
despite OSR ↓

Quantization error ↓

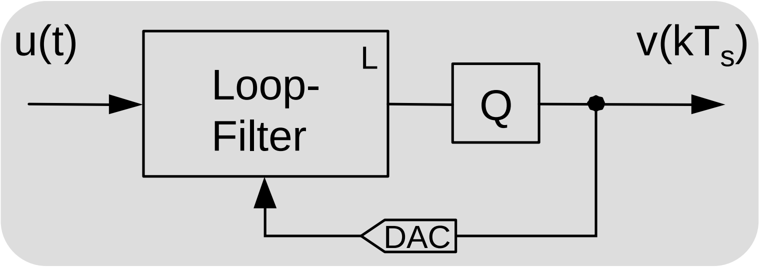
- quantizer / DAC resolution ↑

Loop-filter shaping capability ↑

- cascaded architecture
- order L↑
- better NTFs

Analog building blocks speed and accuracy requirements ↓

- continuous-time loop filter
- single-loop architecture
- single-bit quantizer / DAC



# Single-bit Quantizer / DAC

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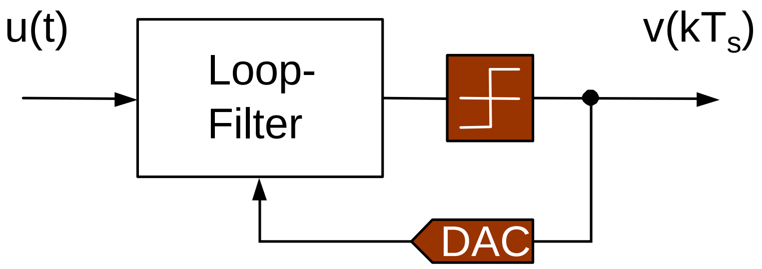
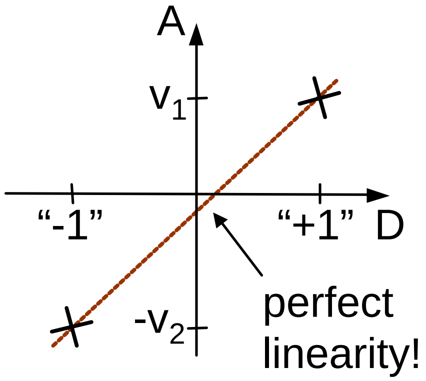


☑ Very simple and fast quantizer (DAC)

☑ Intrinsically linear DAC

1bit DAC I/O-Curve:



☒ Very high quantization error

☒ Poor SNR at low oversampling ratio

# Multi-bit Quantizer / DAC

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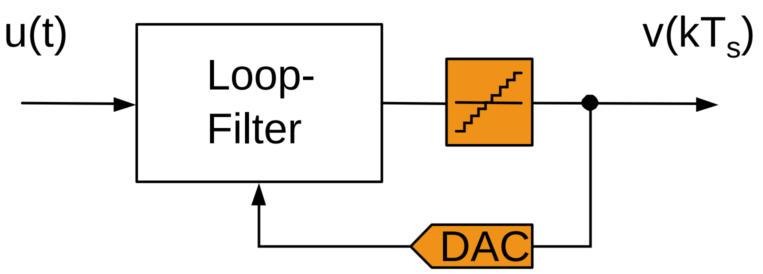
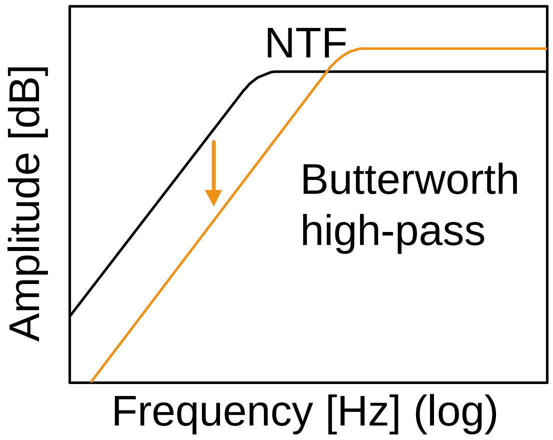


Shaping Improvement:



☑ Quantization error halved for each additional bit

☑ More aggressive NTF allowed

☑ Quantizer non-linearity increases noise level (no distortion)

☒ DAC non-linearity generates distortion

☒ DAC linearity must be as good as overall resolution
→Special linearization techniques required

Linearization Techniques :

# Digital Output Correction

[Larsen88]

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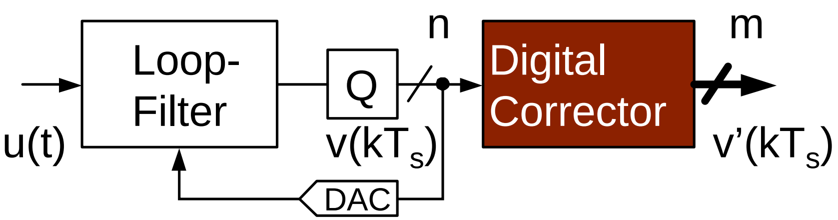
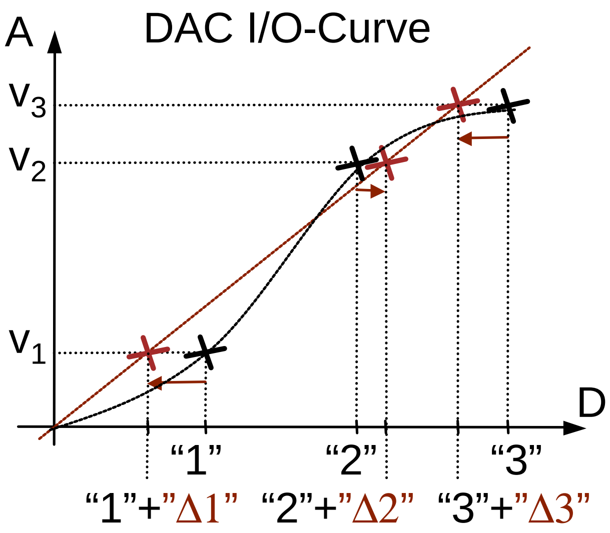


n: quantizer's resolution (2-5 bits)
m: modulator's resolution (13-16 bits)

☑ No overhead in analog part

☒ Large overhead in decimation filter (wide input)

## Calibration Principle:



☒ Calibration time required

☒ Only static errors are corrected (e.g. capacitor mismatch)

# Linearization Techniques : Dynamic Element Matching (DEM)

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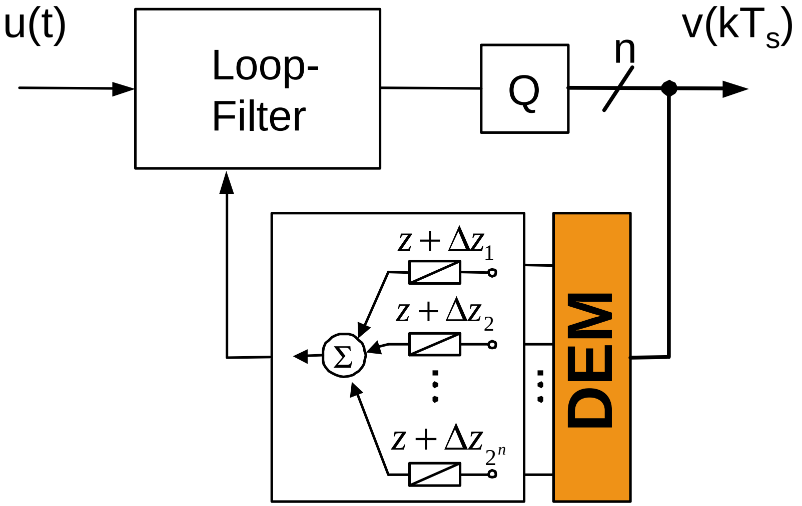
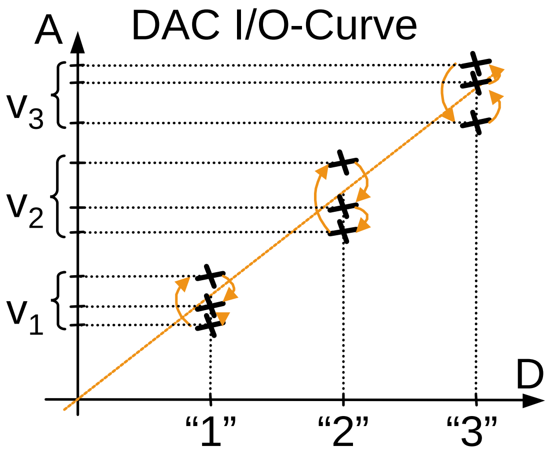


## DEM Principle:



☑ No overhead in decimation filter

☑ Output $v(kT_S)$ always valid

☑ DEM logic can be simple (e.g. DWA)

☒ DAC with equal unit elements required

DEM Example : # Data Weighted Averaging (DWA) [Baird95]

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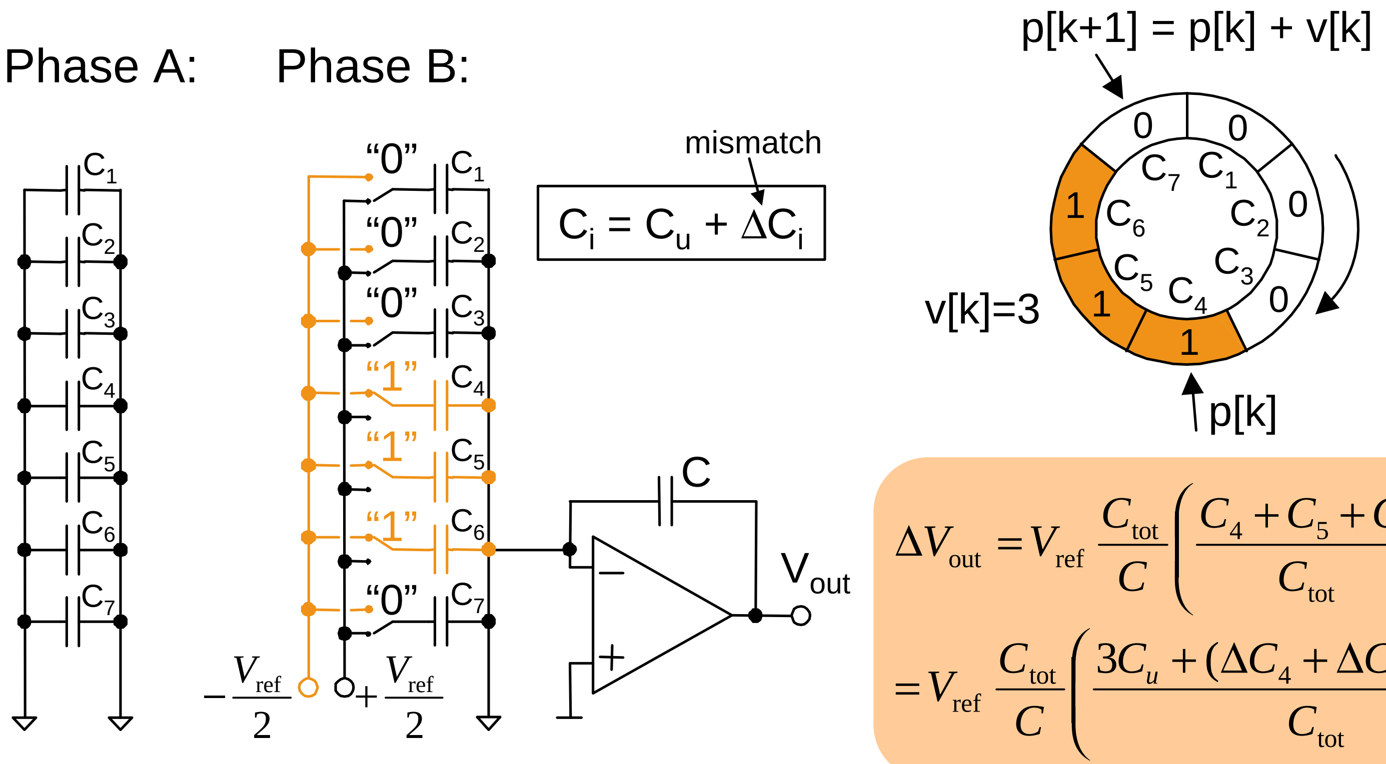
## DWA Algorithm in a 3bit DAC Implemented with SC technique:



$$\Delta V_{out} = V_{ref}\frac{C_{tot}}{C}\left(\frac{C_4 + C_5 + C_6}{C_{tot}} - \frac{1}{2}\right)$$

$$= V_{ref}\frac{C_{tot}}{C}\left(\frac{3C_u + (\Delta C_4 + \Delta C_5 + \Delta C_6)}{C_{tot}} - \frac{1}{2}\right)$$

- ☐ Linearity error is made uncorrelated with digital output
- ☐ First order noise shaping is achieved

# Continuous-Time Loop-Filter

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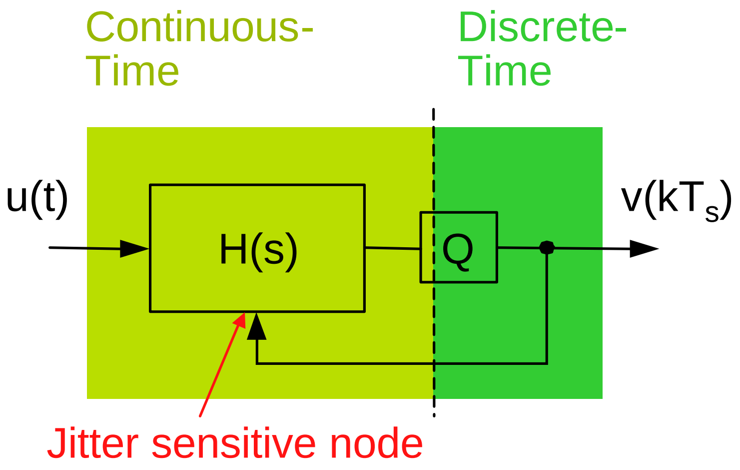


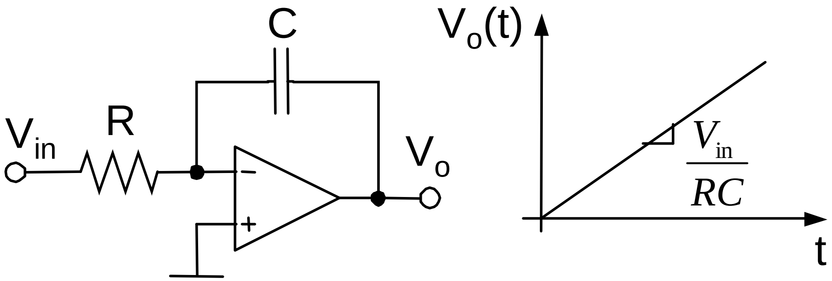
☑ Sampling errors shaped by the loop

☑ Amplifier’s GBW related to 1/RC

☒ Poor coefficient precision (RC)

☒ Clock jitter sensitivity increases with increasing OSR:

Continuous-time RC Integrator:



| | |
|---|---|
| $f_b$ | 1MHz |
| OSR | 32 |
| $A_{max}/V_{ref}$ | 0.7 |
| SNR | 86dB (14b) |

$$s_{jitter} \le \frac{A_{max}/V_{ref}}{2\sqrt{2}\, f_b \sqrt{OSR\, SNR}} = 2.2\,ps$$

[Van Der Zwan96]

# Discrete-Time Loop-Filter

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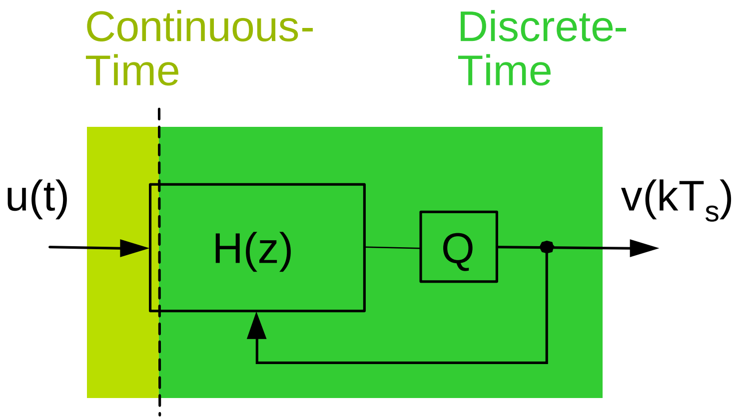


☒ Sampling errors compare to input signal

☒ Amplifier GBW related to settling time (GBW = 5-7 $f_s$)

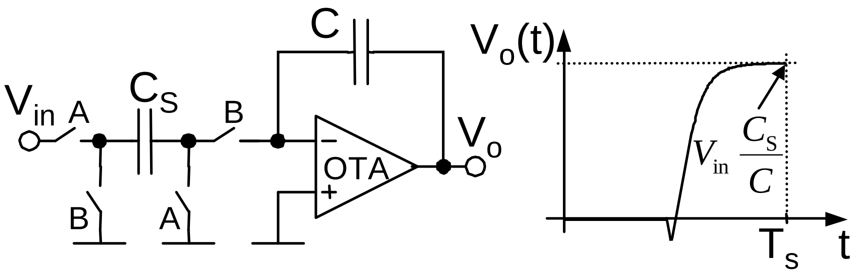
☑ Good coefficient precision ($C_S/C$)

☑ Clock jitter sensitivity decreases with increasing OSR:

| | |
|---|---|
| $F_b$ | 1MHz |
| OSR | 32 |
| SNR | 86dB (14b) |

$$\sigma_{\text{jitter}} \leq \frac{1}{2\pi f_b}\sqrt{\frac{\text{OSR}}{\text{SNR}}} = 45\,ps$$

Discrete-time SC Integrator:



# Single-Loop Modulator

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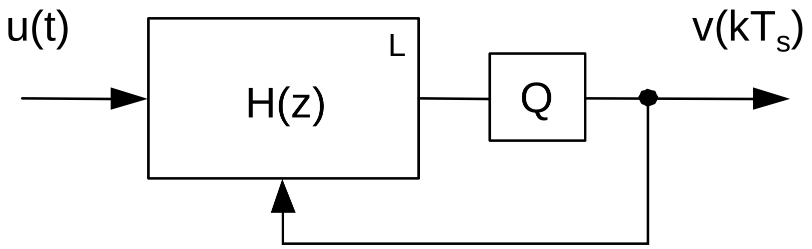

☑ No digital post-processing before decimation filter required

☑ Circuit requirements decrease from first to last stage (Chain of integrators)

☒ Stability condition reduces shaping filter capability at order L>2

# Cascaded Modulator

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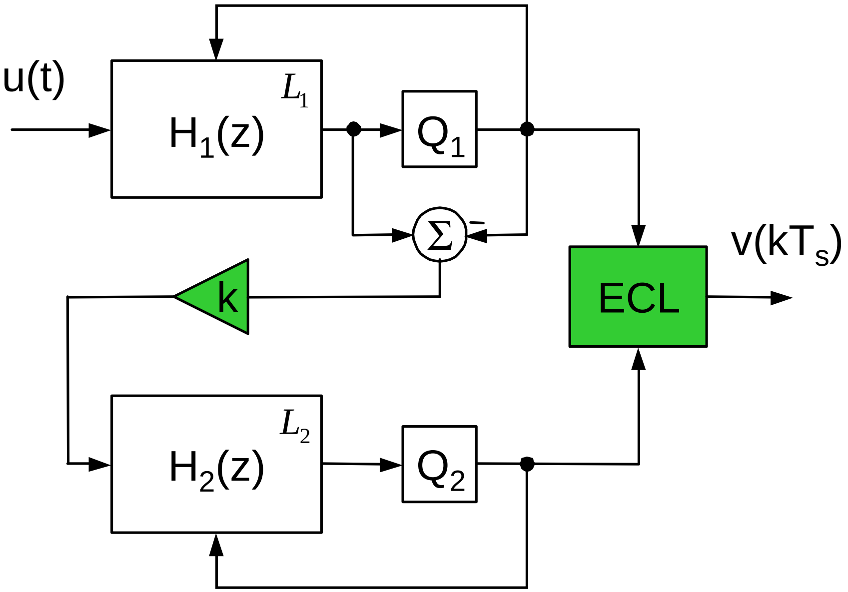

☑ Intrinsically stable

☑ Gain k further improves SNR

☒ Quantization noise of $Q_1$ only theoretically cancelled completely

## Ideal Transfer Functions:

$$\mathrm{ECL} = \frac{1}{k}\frac{1+H_1}{(1+H_1)H_2}$$

$$\mathrm{STF} = \frac{H_1}{1+H_1} \qquad \mathrm{NTF} = \frac{1}{k}\frac{1}{(1+H_1)H_2}$$

☒ Matching requirements between analog and ECL coefficients increase circuit complexity

$Q_1$ error cancellation: $$\Delta q_1 = q_1\left[\frac{1}{1+H_1} - \frac{1}{1+H_1^D}\left(\frac{k}{k^D}\frac{H_2}{1+H_2}\frac{1+H_2^D}{H_2^D}\right)\right] \neq 0$$

# Feedback Filter Topology

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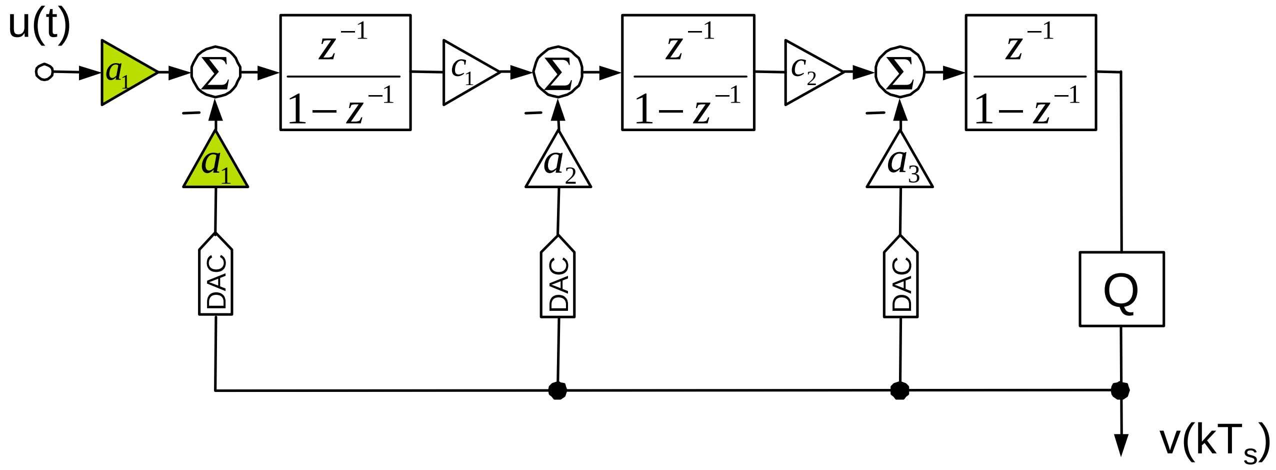
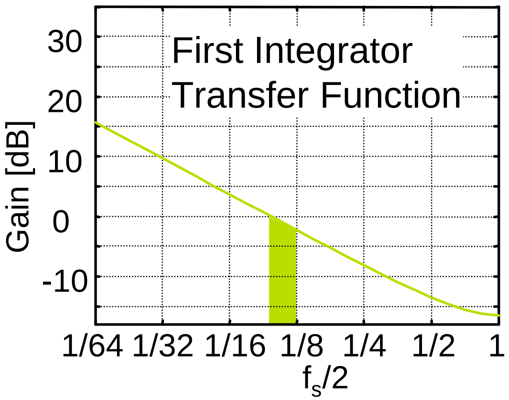


☑ Simple interface between filter and quantizer

☒ “0-delay” feedback requires multiple DACs

☒ Experience shows: 1st integrator has smallest coefficients ($b_1$)
→ bias current scaling difficult at low OSRs

Ex.: $a_1$=0.3, $a_2$= $c_1$=0.8 and $a_3$= $c_2$=2.3 [Geerts00]



# Feed-Forward Filter Topology

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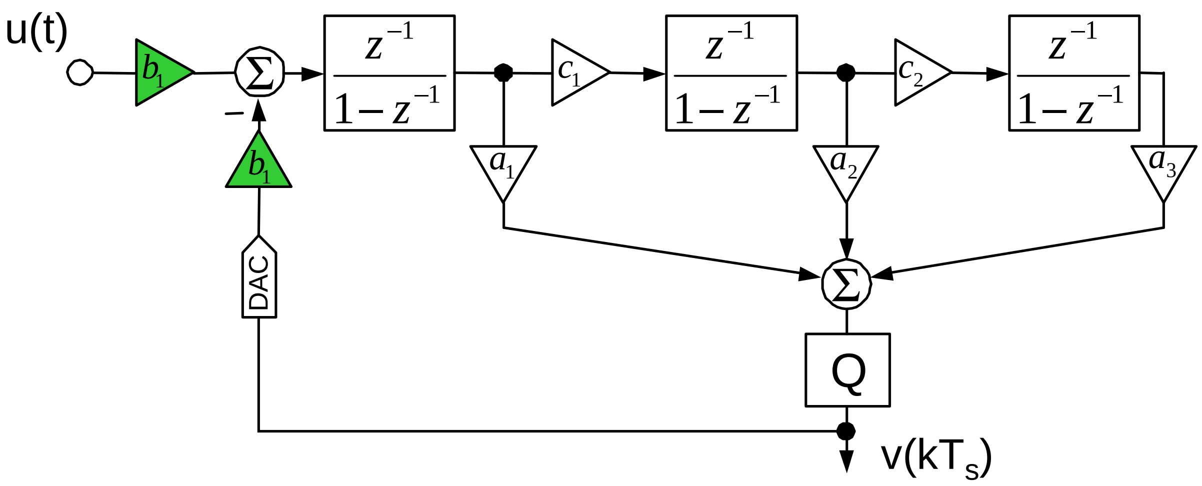
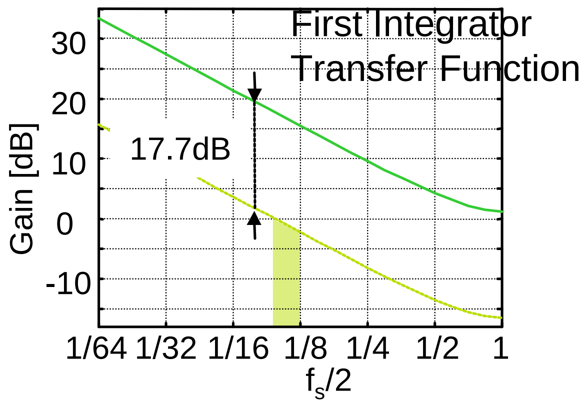


☒ "0-delay" SC-amplifier needed at summing-node (multibit quant.)

☑ Only one DAC required

☑ Experience shows: 1st integrator has largest coefficient ($b_1$)
→ bias current scaling not critical at low OSRs

Ex.: $a_1 = a_2 = a_3 = 1$, $b_1=2.3$, $c_1=0.8$ and $c_2=0.3$ (same NTF as [Geerts00])



# Summary

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- The low OSR of broad-band modulators makes loop-filter design critical.
- Multi-bit quantizer and DEM are the key methods to design high resolution, broad-band ΣΔ modulators.
- Relaxed jitter requirements make discrete-time loop-filter best suited for high speed, high precision modulators.
- Cascaded architecture achieves better noise shaping at low OSR but requires faster amplifiers with higher DC-gain and better capacitor matching.
- Feed-forward topology is better suited for broad-band modulators because it allows the amplifier power consumption to be scaled more aggressively.

# Design Example

[balmelli00]

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  - *-architecture*
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  - *-input stage*
  - *-T-circuit*
  - *-quantizer*
  - *-amplifier*
  - *-comparator*
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  - *-SNR, SNDR*
  - *-summary*
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## A 50mW 14bit 2.5MS/s ΣΔ Modulator for Communication Applications

# Application

Bandwidth: ~1MHz (SSB)
Data rate: 750-1500kbit/s (x3)
Not yet standardized

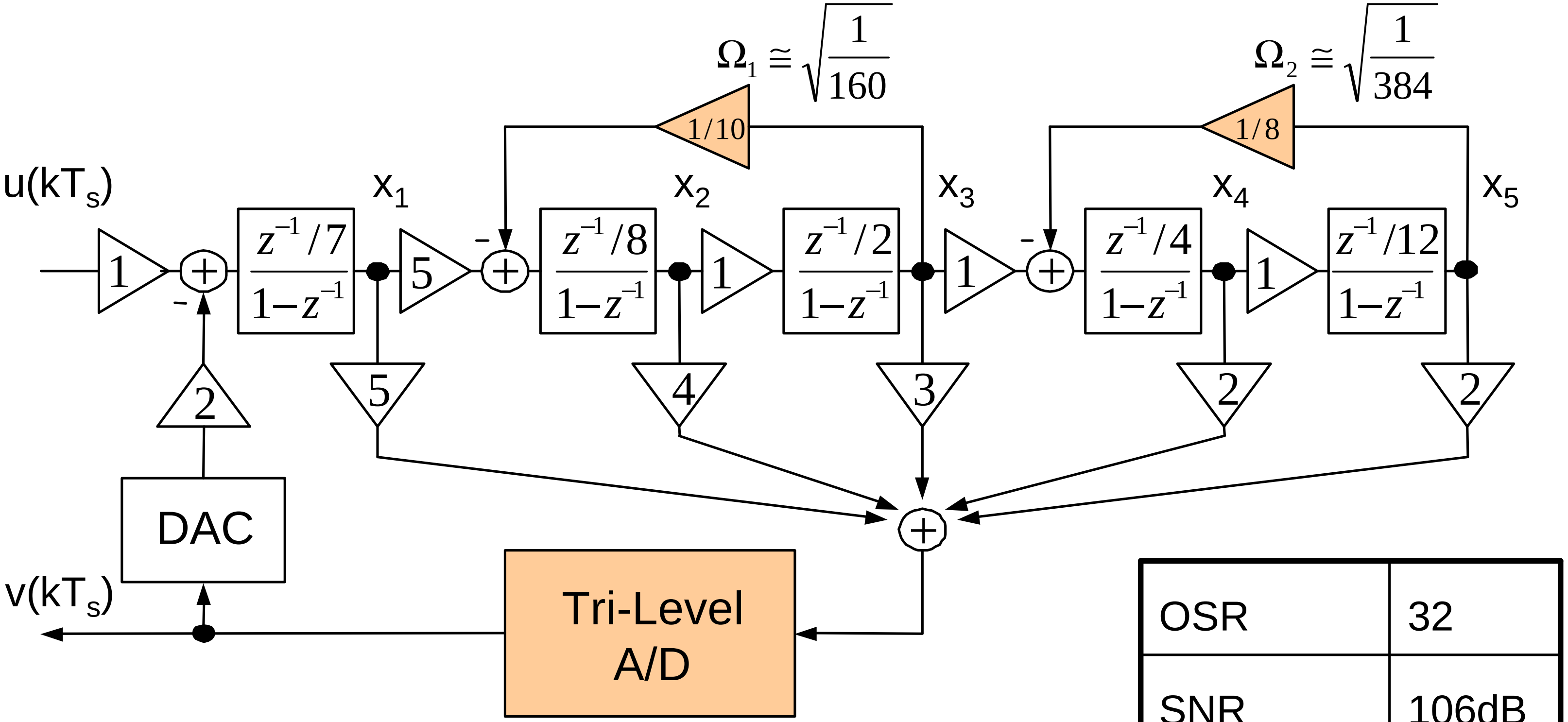
Bandwidth: 1.1MHz (BB)
Data rate: 2-9Mbit/s

Bandwidth: ~800kHz (DSB)
Data rate: 1.152Mbit/s

# Why Low Power ?

- ☐ Longer battery lifetime (DECT, ~ADSL)
- ☐ Heat removal capability limits modem density in central office (ADSL)
- ☐ USB bus-powered devices can only sink limited maximum power (DECT, ADSL)

# Modulator Architecture



| | |
|---|---|
| OSR | 32 |
| SNR | 106dB |
| $A_{max}$/ref | 1 |
| max($x_i$/ref) | 0.4 |

- ☐ SNR boosted by 17dB using tri-level quantizer
- ☐ Frequency $\Omega_1$ and $\Omega_2$ selected to minimize in-band noise

# SC Circuit Implementation

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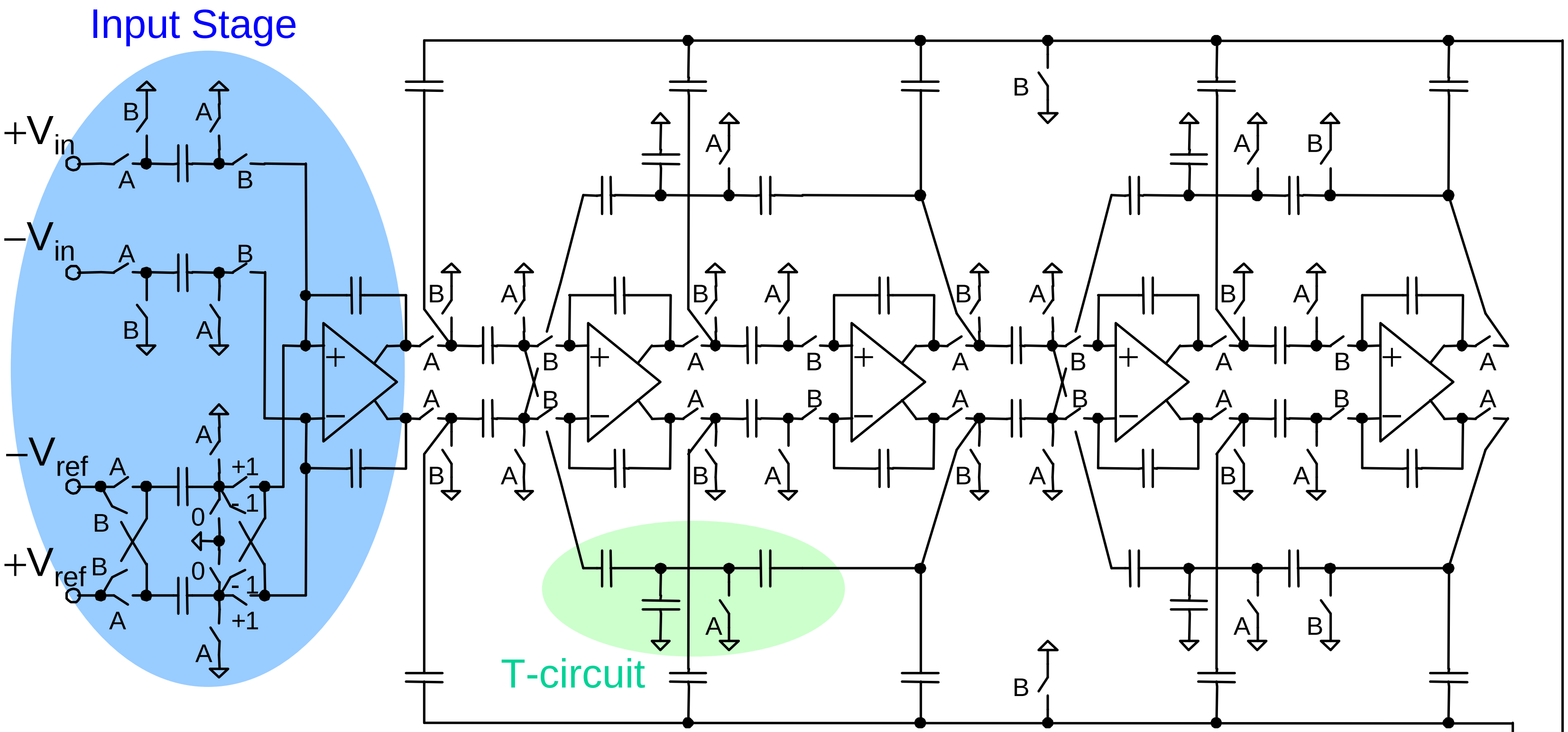
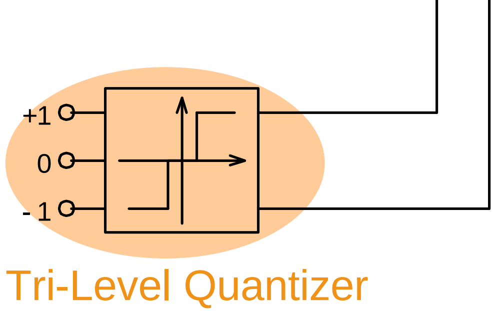
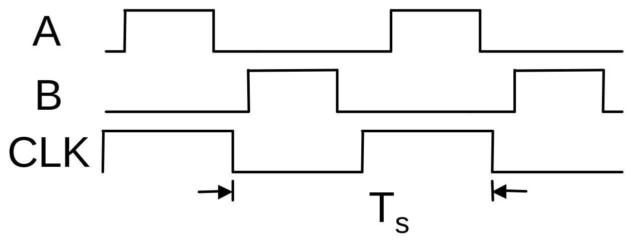




Tri-Level Quantizer



| | |
|---|---|
| $T_s$ | 12.5ns |
| $2V_{ref}$ | 1.6V |

# Input Stage

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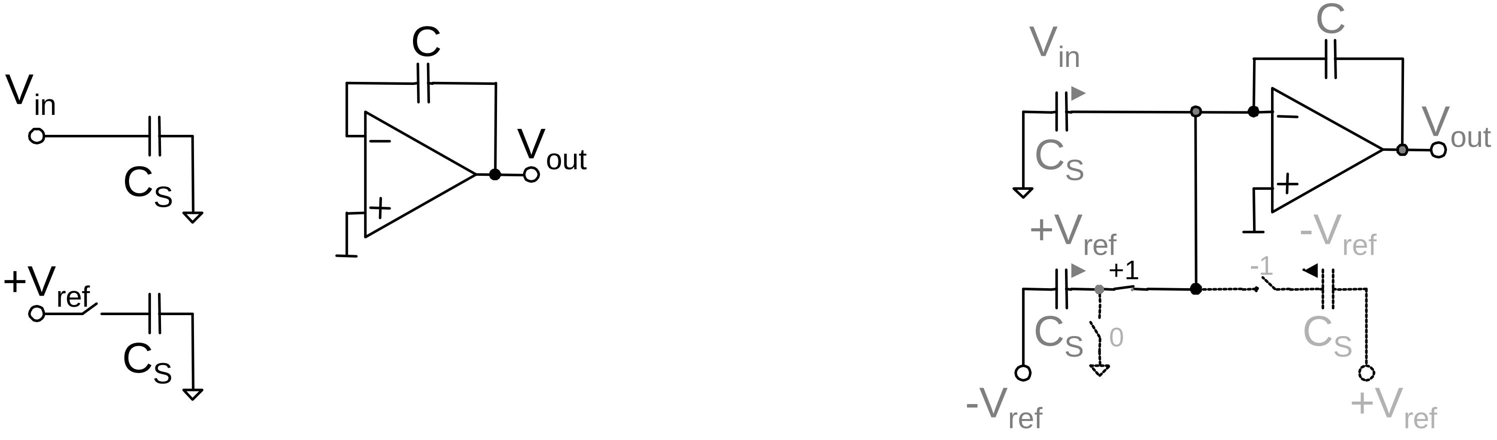
Phase A: Phase B:



$$\Delta V_{out} = \left(V_{in} + (+1/0/-1)\cdot 2V_{ref}\right)\frac{C_S}{C}$$

- ❑ No supplementary capacitor needed to implement 0 state
- ❑ Gain in feedback path implemented with cross-coupled reference
- ❑ $C_S$=0.5pF selected to achieve SNR=87dB (KT/C-noise)

# T-Circuit

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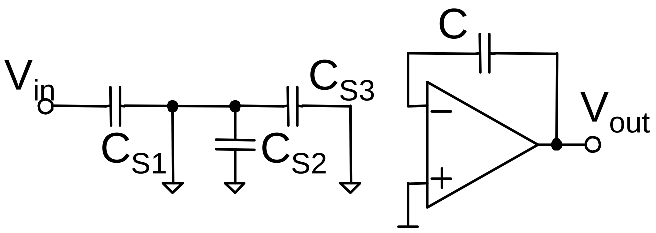
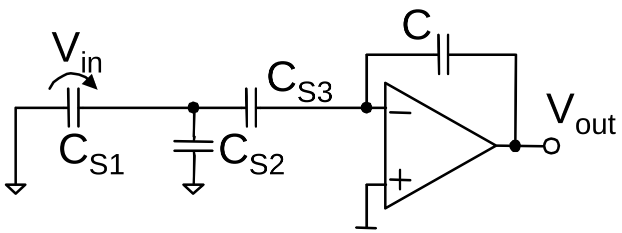
Phase A:



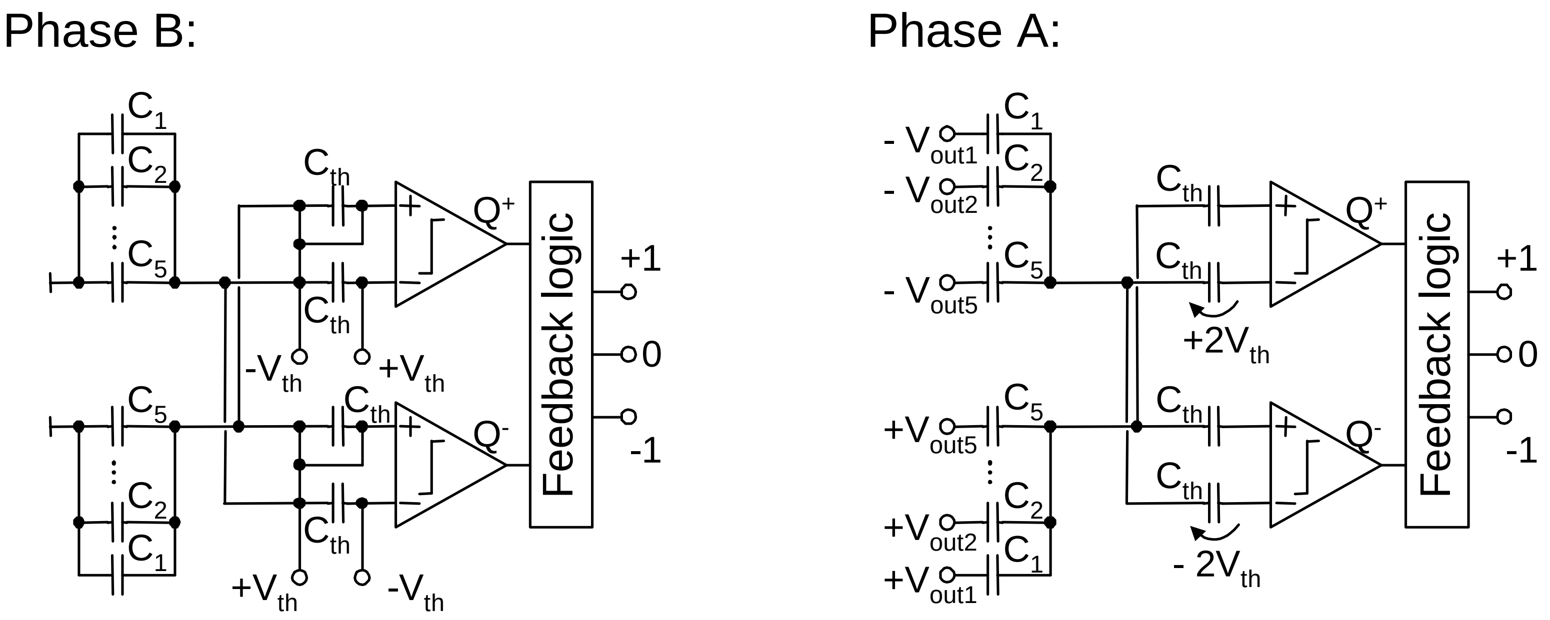
Phase B:



$$\Delta V_{out} = \frac{C_{S1}}{C_{S1}+C_{S2}+C_{S3}} \frac{C_{S3}}{C} \cdot V_{in}$$

☐ Small coefficient implemented with big (more precise) capacitors

# Quantizer



$$Q^{-} = \mathrm{sgn}\left(2\sum_{i=1}^{5}\frac{C_i}{C_{\mathrm{tot}}}V_{\mathrm{out}\,i} + 2V_{\mathrm{th}}\right)$$

$$Q^{+} = \mathrm{sgn}\left(2\sum_{i=1}^{5}\frac{C_i}{C_{\mathrm{tot}}}V_{\mathrm{out}\,i} - 2V_{\mathrm{th}}\right)$$

$$C_{\mathrm{tot}} = C_1 + C_2 + C_3 + C_4 + C_5$$

- Input summing node implemented with passive components

# Amplifier

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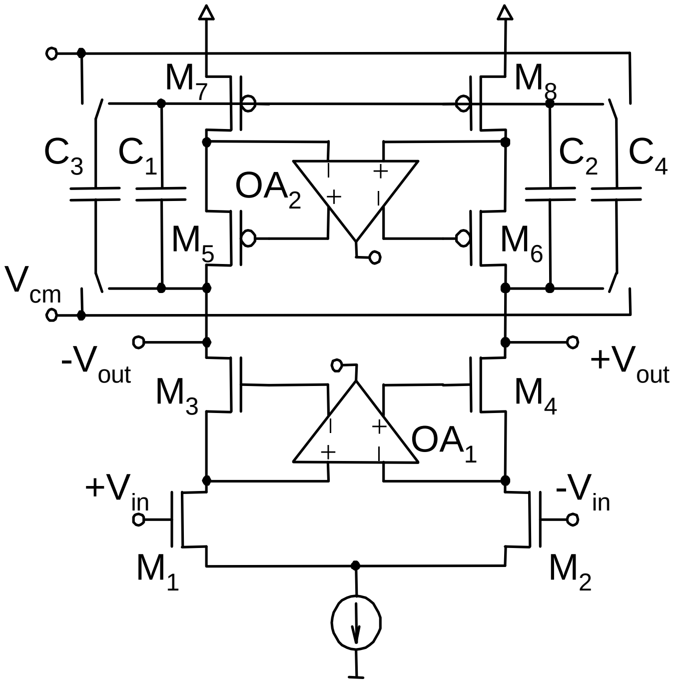

| | |
|---|---|
| $GBW_{loop}$ | 800MHz |
| $A_{dc}$ | 110dB |
| $I_{tot1}$ | 8mA |
| $I_{tot}$ scaling | 1, 1/3, 1/6, 1/6, 1/6 |

- High speed and DC gain achieved with regulated cascode, telescopic OTA
- SC common-mode feedback controls PMOS transistors (M7, M8)
- $OA_1$ and $OA_2$ are folded cascode amplifiers, with PMOS and NMOS input, respectively

# Comparator

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  - *-input stage*
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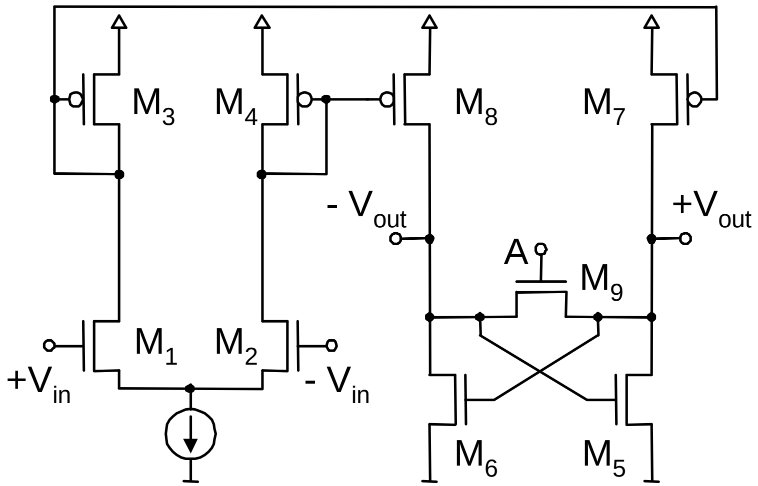
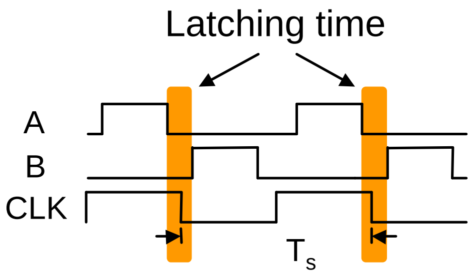
  - *-quantizer*
  - *-amplifier*
  - *-comparator*
  - *-output signal*
  - *-SNR, SNDR*
  - *-summary*
- Conclusion



| | |
|---|---|
| $I_{tot}$ | 325µA |
| $\tau_{latch}$ | <1ns |



❑ Comparator latched at end of phase A

❑ Digital output valid at beginning of phase B

❑ Latch current limited by transistors $M_7$ and $M_8$ (no current peaks)

# Measurements: Output Signal Spectrum

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  - *-comparator*
  - *-output signal*
  - *-SNR, SNDR*
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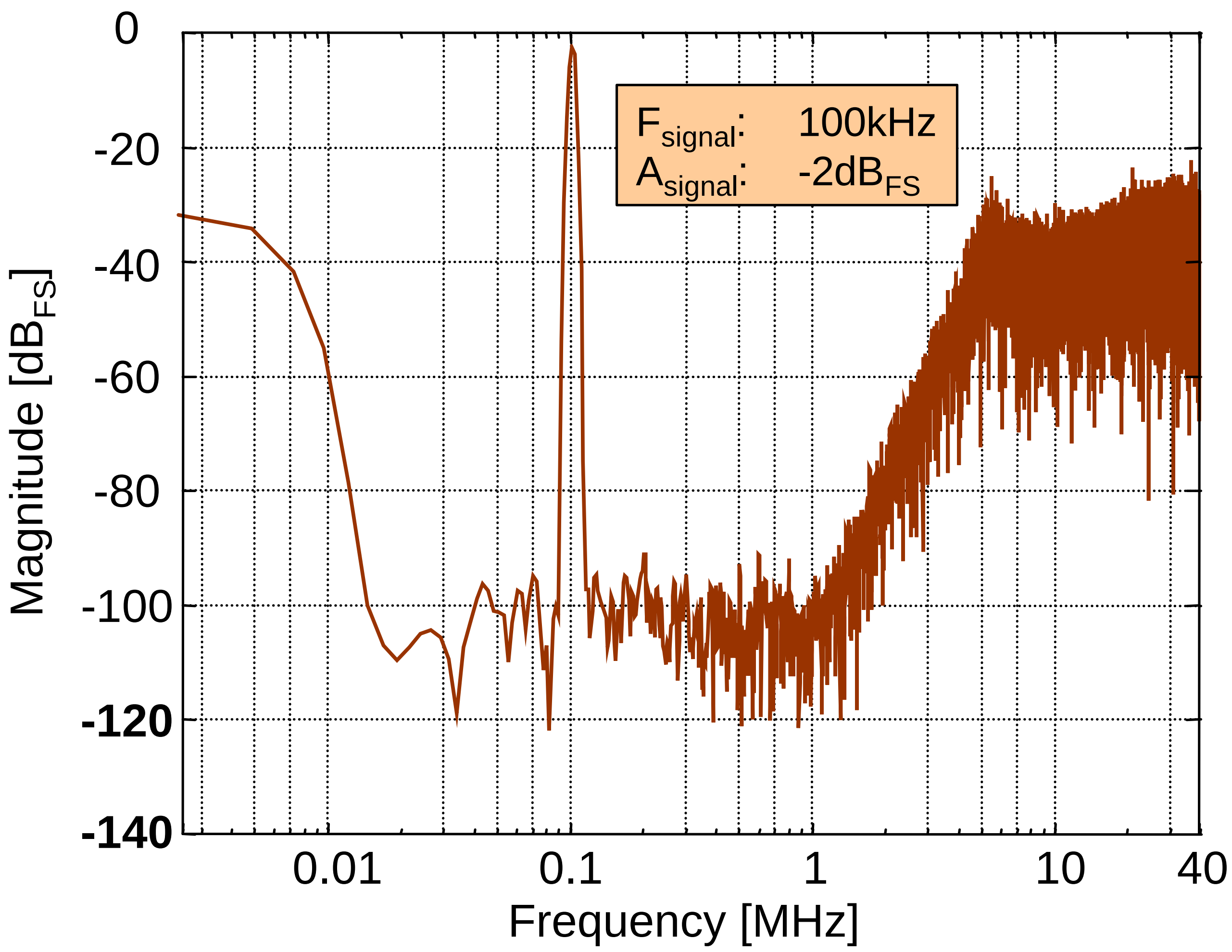
- Conclusion



# Measurements: SNR, SNDR, DR

- Outline
- Introduction
- Architectures
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  - *-amplifier*
  - *-comparator*
  - *-output signal*
  - *-SNR, SNDR,…*
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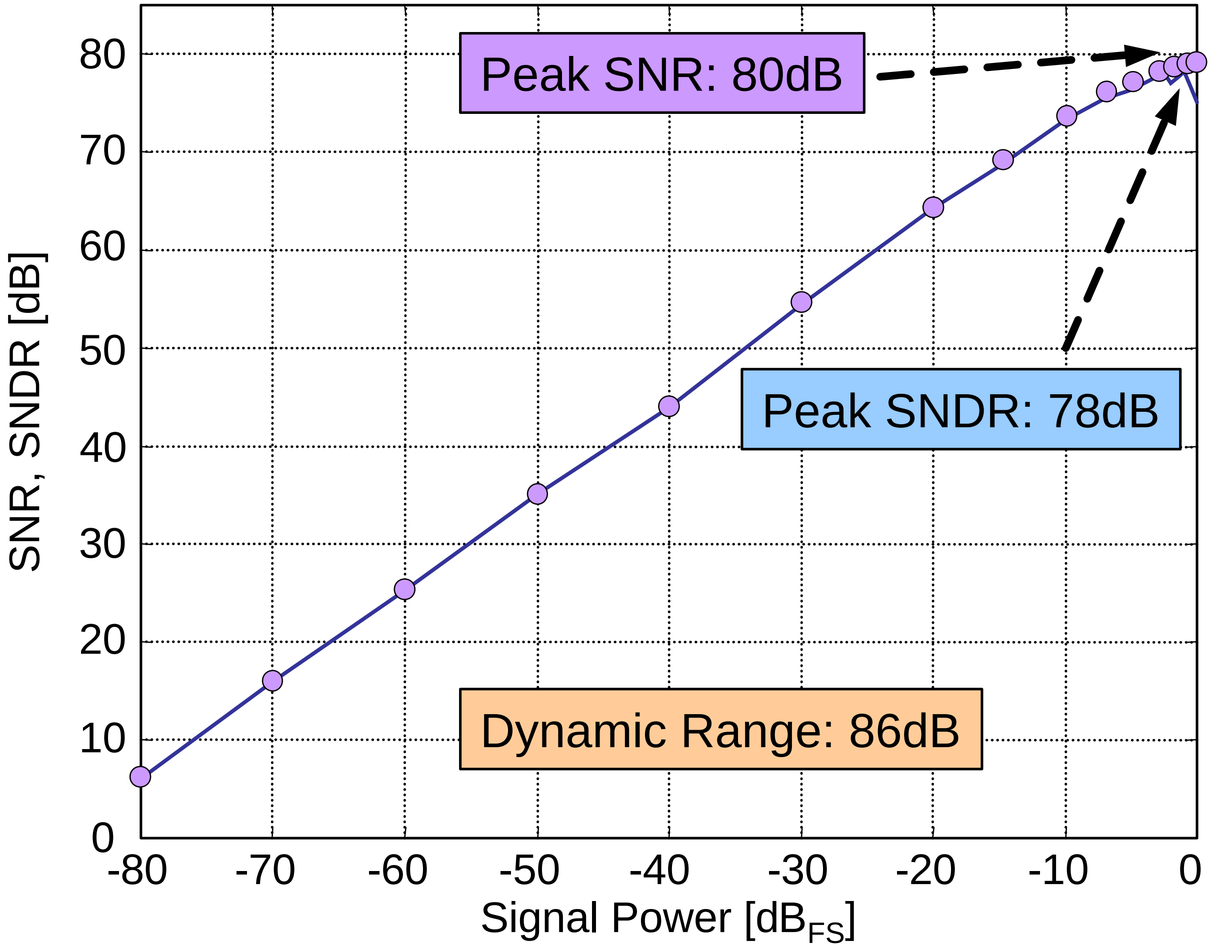
- Conclusion



# Performance Summary

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  - *-low power*
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  - *-SC modulator*
  - *-input stage*
  - *-T-circuit*
  - *-quantizer*
  - *-amplifier*
  - *-comparator*
  - *-output signal*
  - *-SNR, SNDR*
  - *-summary*
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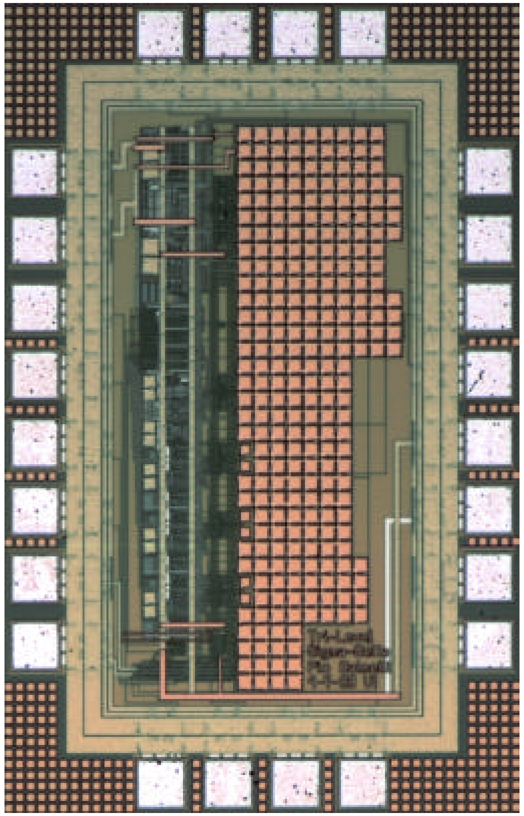
## Performance Table:

| | |
|---|---|
| Clock frequency | 80 MHz |
| Oversampling ratio | 32 |
| Signal bandwidth | 1 MHz |
| Dynamic Range | 86 dB |
| Peak SNR | 80 dB |
| Peak SNDR | 78 dB |
| Power consumption | 50 mW |
| Supply voltage | 2.5 V |
| Input voltage range | 3.2 Vpp |
| Reference voltage | 1.6 V |
| Process | 0.25 µm CMOS SP 6M |
| Capacitors | M1-M6 Sandwich |
| Chip size | 1.1 mm$^2$ |

## Die Photo:



An improved version of this circuit that consumes only 33mW and includes the digital decimation filter will be presented at ISSCC 2002.

# Conclusion

☐ Design options for the implementation of a ΣΔ modulator have been presented. Best architecture choices to achieve high resolution despite low OSRs have been shown.

☐ The considerations done in the first part have been used to find an optimal architecture for a low-power broad-band modulator.

☐ The realization of the different analog building blocks has been sketched and explained. Performance and measurements of the final circuit have been given.

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