High-Speed ΣΔ D/A Converters

Pier Andrea Francese, IIS, ETH
Zürich

22. 10. 2001

Outline

❶ D/A Converters
- DAC basics
- Why ΣΔ DACs?

❷ Broadband ΣΔ DAC
- Modulator requirements
- Dual-truncation MASH
- Semi-digital FIR filter
- Hybrid FIR/IIR filter

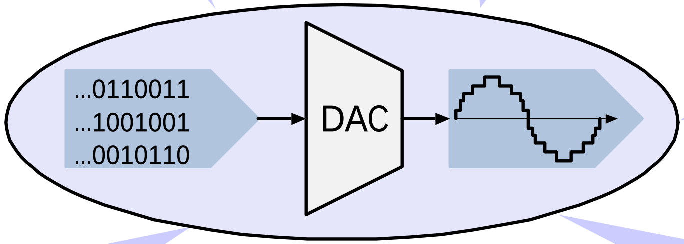
❸ MADBRIC ΣΔ DAC
- Design overview
- Simulation results

🕛 Summary

❶

D/A Converters

DAC Categories



Implementation

- R-2R Ladder
- Voltage Division
- Charge Redistribution
- Current Steering

Frequency conversion

- Nyquist-rate
- Oversampled
- Sigma-Delta

Amplitude conversion

- Flash
- Algorithmic (or cyclic)
- Pipelined

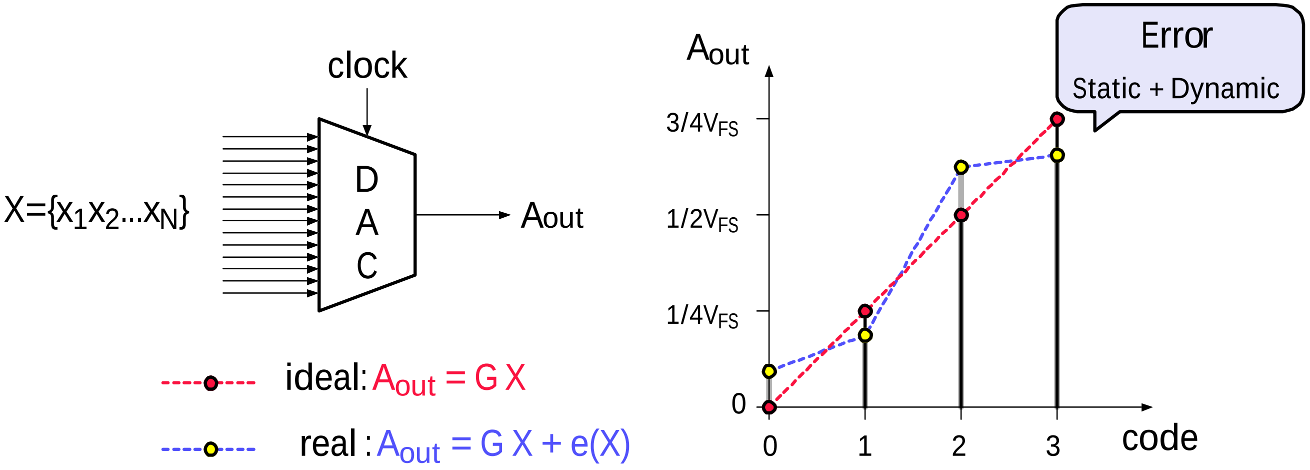
Coding scheme

- Binary
- Thermometer
- Segmented

DAC linearization technique

1. Trimming
2. Dynamic Element Matching
3. Pulse-Width Modulation
4. Self-calibration

DAC Basic Operation



ideal: $A_{out} = G\,X$

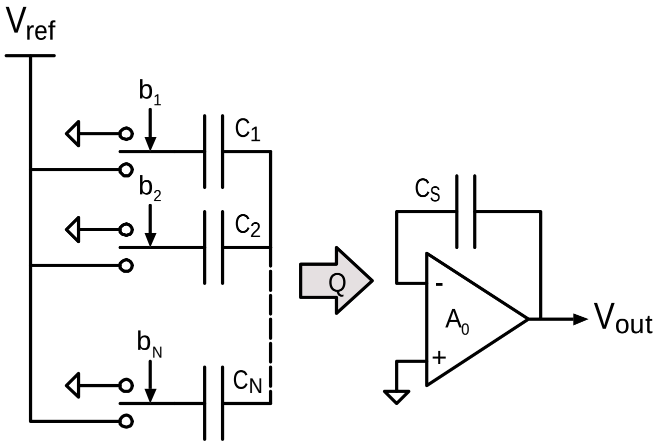
real : $A_{out} = G\,X + e(X)$

Static Performance:
- INL
- DNL
- Gain
- Offset
- Monotonicity

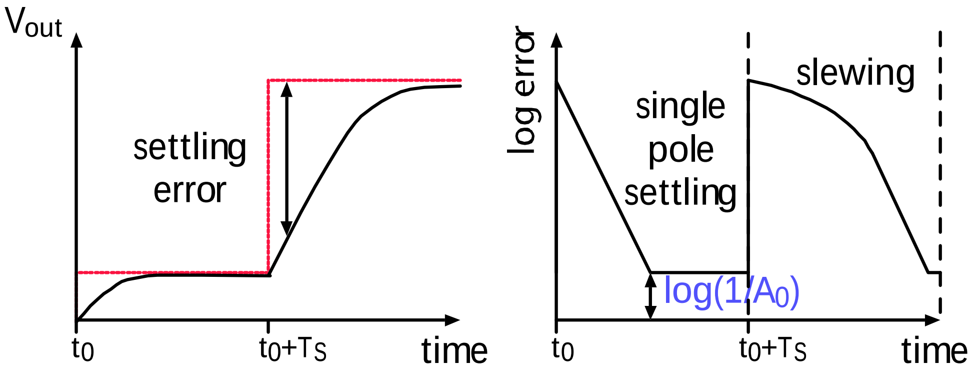
Dynamic Performance:
- SNR
- SFDR
- Settling errors
- Code glitches
- Sampling jitter
- Clock feedthrough

☐ 14-bit accuracy and1.8V full differential swing: $\text{error} \leq \frac{1}{2} \cdot \text{LSB} = 2^{-15} \cdot 1.8\text{V} \cong 55m\text{V}$

Example → Charge Redistribution DAC



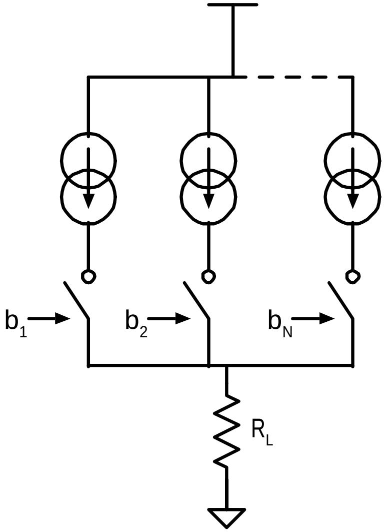
- ❑ Technology
  - 0.1% matching → ~10 bits
- ❑ OTA GBW
  - Conversion speed → $f_{GBW} = 5..7 f_S$
- ❑ Switches and OTA noise
  - Dynamic range → $\overline{v_n^2} \propto \dfrac{kT}{\sum C_i}$

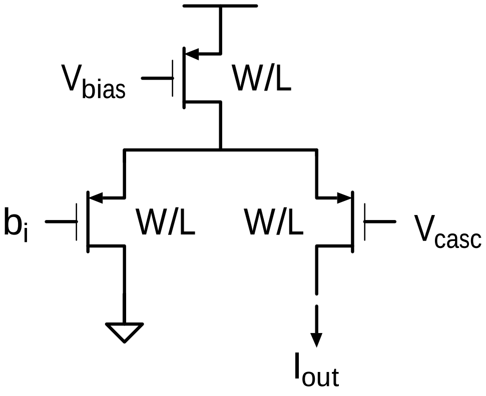


- ❑ Signal-dependent nonlinearities
  - OTA slewing, limited gain and CMRR
  - Switches ON resistance
  - Clock feedthrough
  - Glitches and sampling jitter

Example → Current Steering DAC

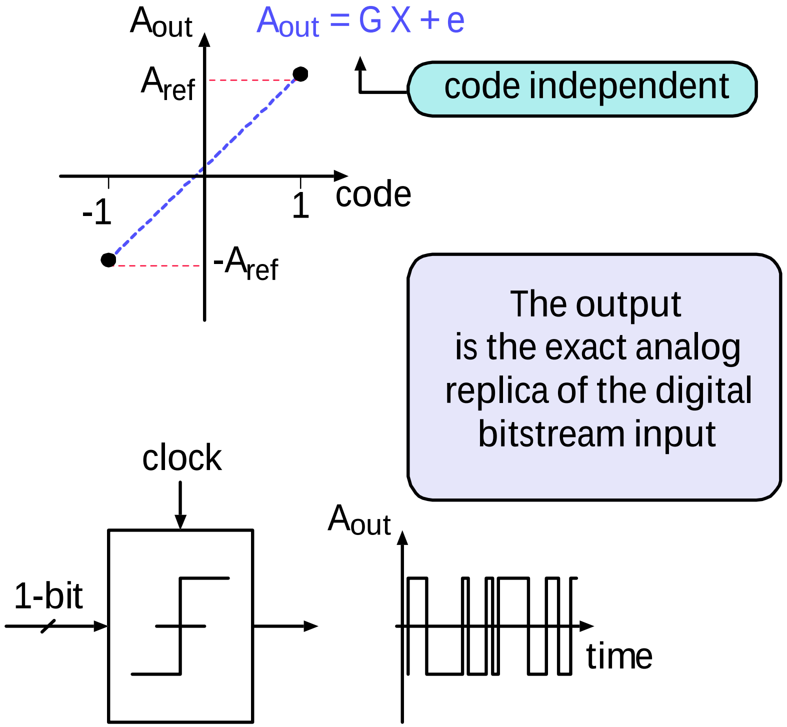
- Suitable for high-speed DACs
  - currents are easy to sum and switch fast
  - all currents can be directly switched to the load → no high bandwidth output buffer
- Power efficient
- Implementation requires only digital CMOS processes
- Successful self-calibration techniques reported [Wouter, JSSC, Dec. 1989]





- Cascoded current source design trade-offs (I_{out}= constant for a fixed load)
  - Maximize
    - pole frequency: $g_m/C_{gs} \sim 1/\sqrt{W\cdot L^3}$
    - output resistance: $r_o^2 g_m \sim \sqrt{W\cdot L^3}$, $r_o \sim L$
  - Minimize
    - Noise: $\overline{I_n^2} \sim g_m \sim \sqrt{W/L}$
    - Mismatch ~ $1/(W\cdot L)$

Single bit DAC



code independent

The output is the exact analog replica of the digital bitstream input

- ✓ Inherently statically linear:

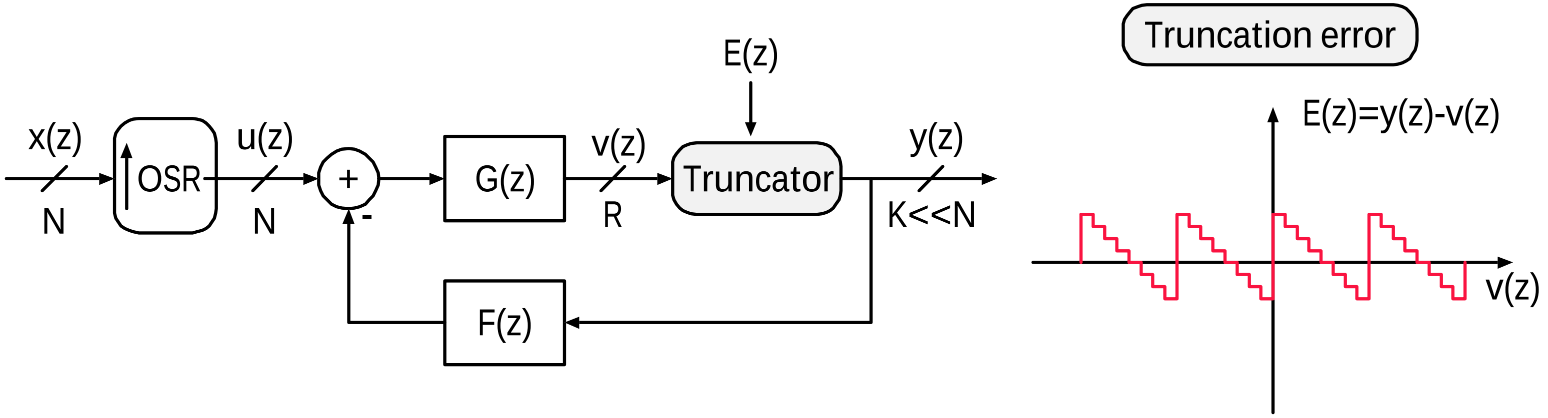
  $V_{out}= G X$

- ✓ Ideally not affected by signal dependent settling errors in a fully differential implementation and a proper switching scheme (e.g. R2Z)

❑ Application

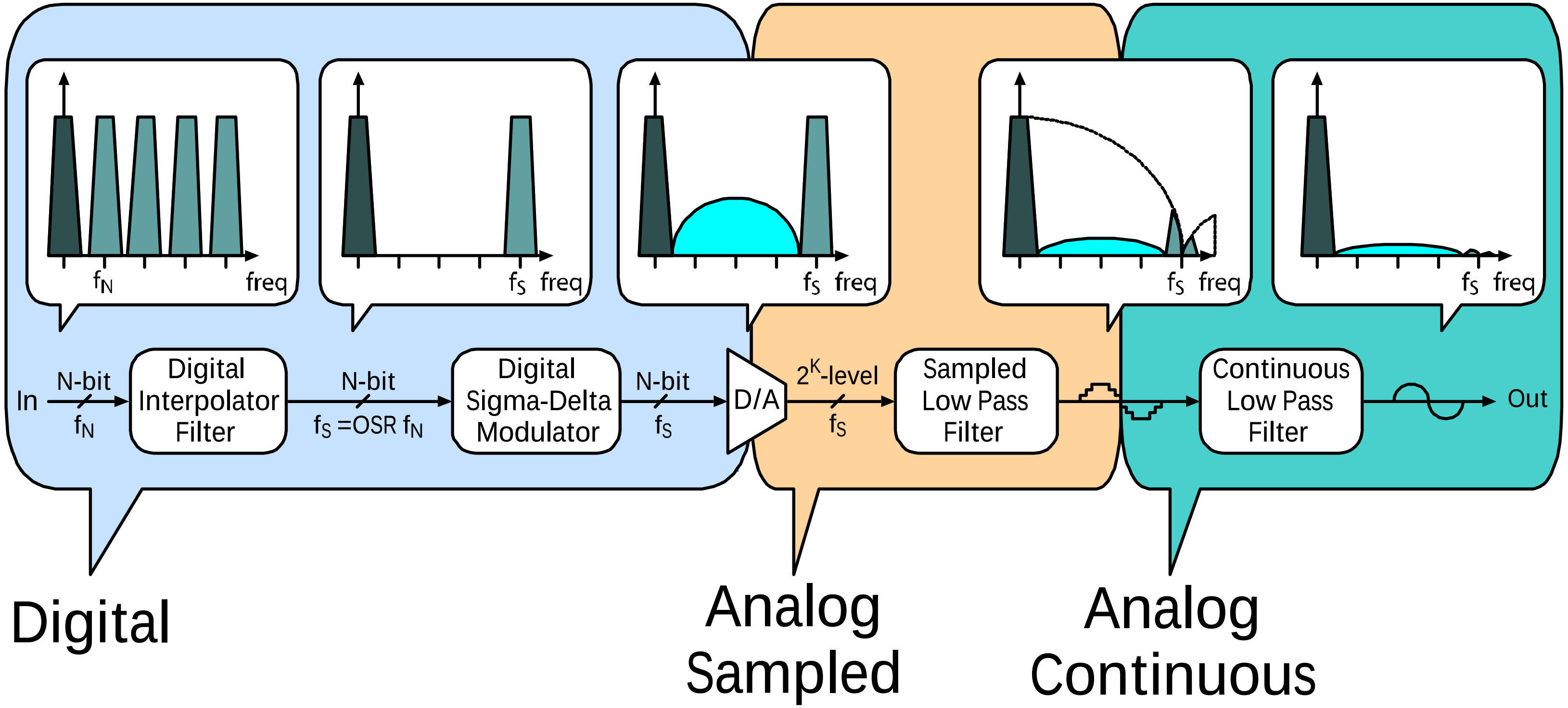
- PWM Converters: M-level signal @ $F_S \leftrightarrow$ 2-level signal @ $M \bullet F_S$
- ΣΔ Converters

Digital ΣΔ Modulation Principle



- ❑ Oversampling and feedback are used to achieve high DAC linearity and resolution
- ❑ The oversampled N-bit input signal is modulated into a much smaller number of bits K. Ideally K = 1 for the best linearity
- ❑ The extended frequency space from oversampling is efficiently used to accommodate the high pass filtered error introduced by the truncation
- ❑ Low number of bits DACs are easier to design, test and linearize

ΣΔ DAC Block Diagram



- ❑ The modulator essentially defines the main requirements for the other blocks. Main design difficulty lies in the reconstruction filter:

  ΣΔ DAC → Filter Design Problem

- ❑ Definition of a proper cost function necessary for comparison of different architectures

Digital ΣΔ Modulators

☺ WYSIWYG → What You Simulate Is What You Get

Specifications

- Bandwidth
- SNR
- Stable dynamic range

Parameters

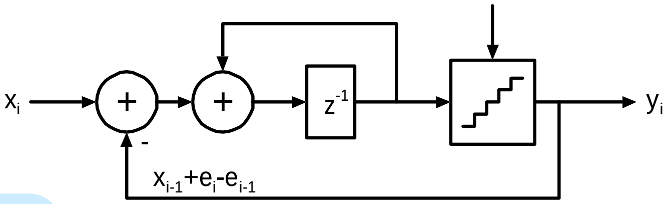
- OSR
- DAC nr. of bits
- Modulator order
- NTF zeros
- Word lengths

?

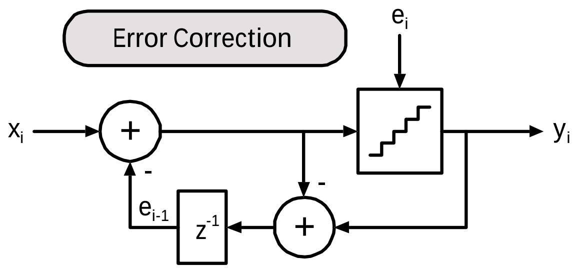
Topologies

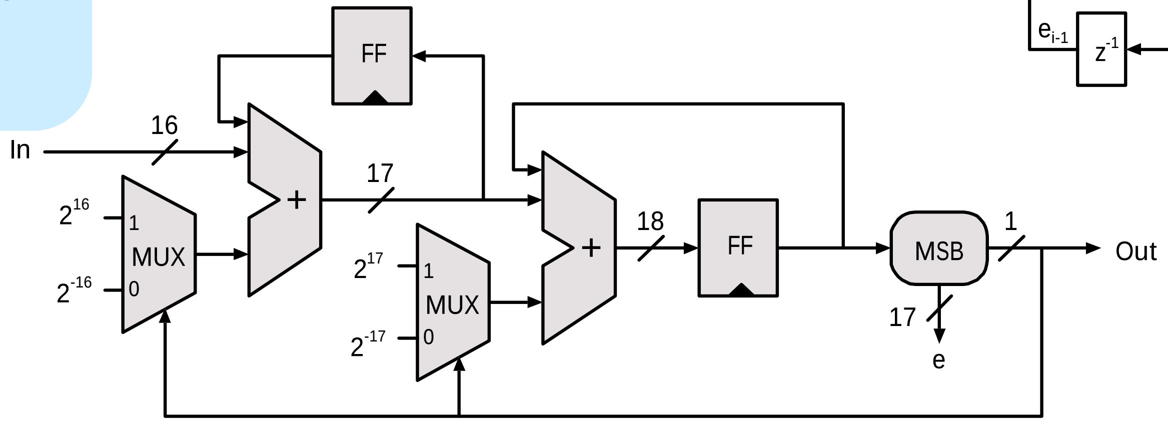
- Sigma-Delta
- Error Correction

Sigma-Delta



Error Correction





2^{nd} order loop

Analog Reconstruction Filters

- ☐ Switched Capacitor
  - Pros & Cons
    - ✓ Linearity – Precision - Versatility (IIR/FIR) – Reproducibility
    - ✗ DR limited by kT/C and OTA noise - High OTA GBW, PM, SR… - Signal replicas
  - Design issues
    - OTA design - Capacitor matching & bottom plate parasitic – Low VDD switches
- ☐ Switched Current
  - Pros & Cons
    - ✓ High Speed – Digital CMOS Process – Low Voltage – Good semi-digital IFIR
    - ✗ Linearity – Precision - DR limited by kT/C - Signal replicas
  - Design issues
    - MOS matching – Good current cells (automated design ?)
- ☐ Continuous Time
  - Pros & Cons
    - ✓ High Speed – Low Power – Low Voltage – No replicas
    - ✗ Linearity – Precision – Reproducibility – Clock jitter
  - Design issues
    - Linear matched resistors – GmC stages

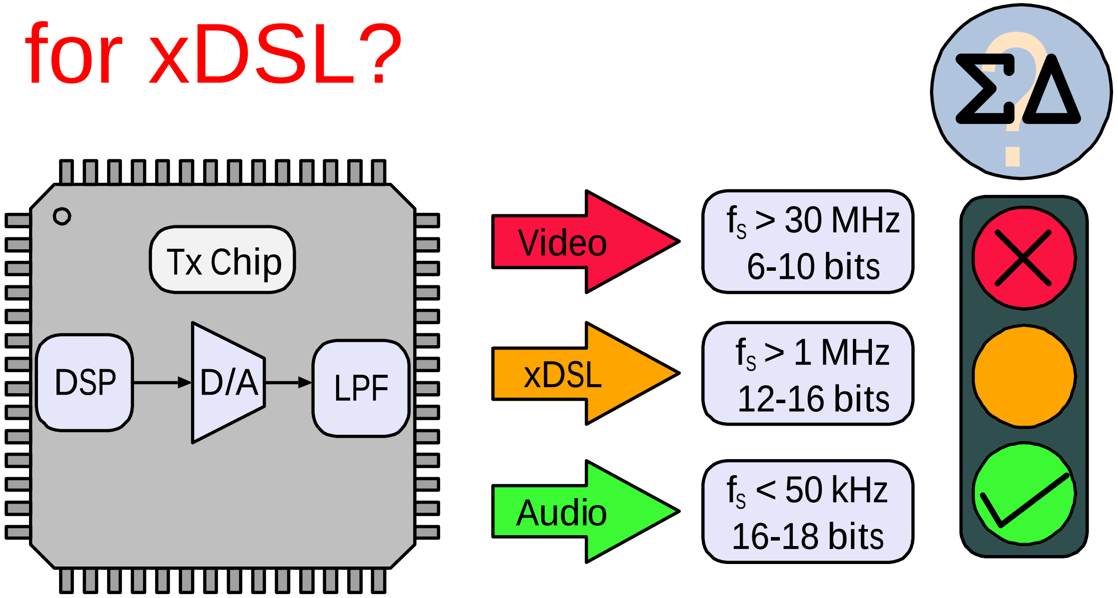
❷

Broadband ΣΔ DACs

Broadband ΣΔ DAC Design Challenges

- Use of standard CMOS technology (matching < 0.1%)
- Wide signal bands (1..10MHz)
- In-band and out-of-band noise requirements (transmission mask specification)
- High resolution (12-14 bits) and signal integrity (SFDR > 70dBc)
- Power dissipation
- Optimal system partitioning and design methodology
- Design robustness and testability

ΣΔ DAC for xDSL?



☹ No established D/A conversion architecture for xDSL applications

Wide range of specifications

↓

Comparison criteria ?

Type	Upstream data rate	Downstream data rate
ADSL	16 kbps to 640 kbps	1.544 Mbps to 9 Mbps
VDSL	3 Mbps	25 Mbps
HDSL	1.5 Mbps	1.5 Mbps
IDSL	144 kbps	144 kbps
SDSL	1.5 Mbps	1.5 Mbps

Designing Broadband ΣΔ DAC Modulator

- ☐ Low Oversampling Ratio:

$$f_b = 1..5\text{MHz} \Rightarrow \text{OSR} = 8..16$$

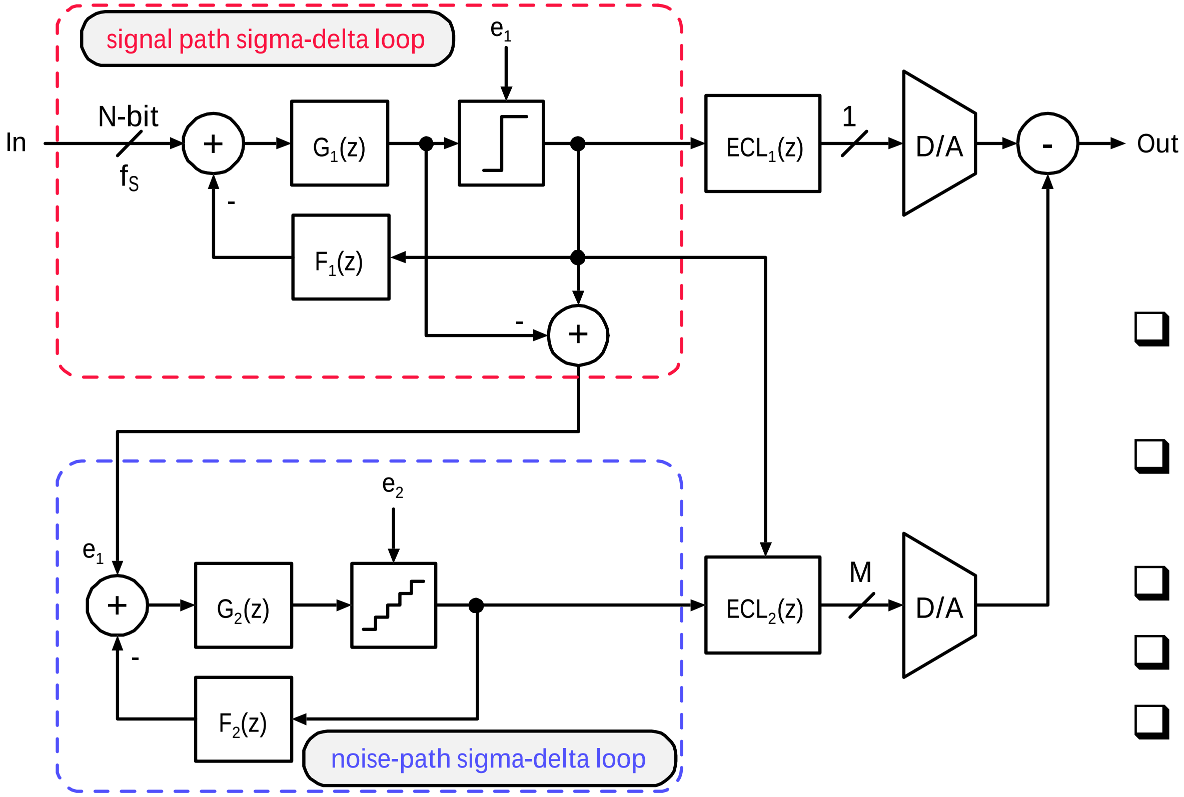
$$\left.\begin{array}{l} f_b = 5\text{MHz} \\ \text{OSR} = 12 \end{array}\right\} \Rightarrow f_S = 120\text{MHz}$$

- ☐ Multibit or MASH:

$$\text{SNR} = 86\text{dB} \Rightarrow 4^{\text{th}}\text{order}: \begin{cases} 1-\text{bit quantizer} \rightarrow \text{OSR} = 32 \\ 5-\text{bit quantizer} \rightarrow \text{OSR} = 10 \end{cases}$$

- ☐ e.g.
  - [Gattani, JSSC, Dec. 2000]
    - 4th MASH, 2-bit quantizer, OSR = 31, f_b=400kHz, SC-DAC
  - [Falakshahi, JSSC, May 1999]
    - 4th, 6-bit quantizer, OSR = 12, f_b=5MHz, Current Steering-DAC

Dual-Truncation MASH architecture



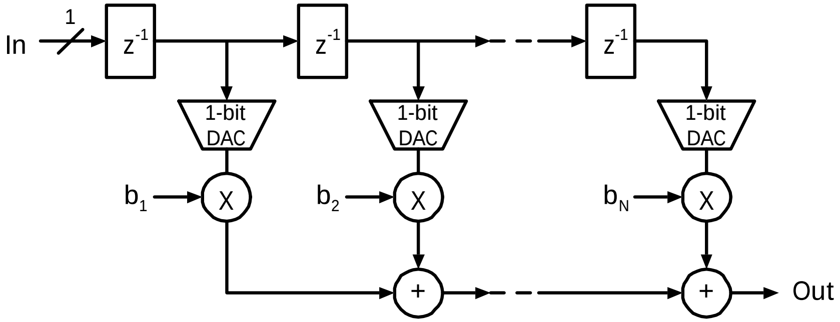
$$STF_2(z) = ECL_1(z)$$

$$STF_{out}(z) = STF_1(z)STF_2(z)$$

$$NTF_{out}(z) = NTF_1(z)NTF_2(z)$$

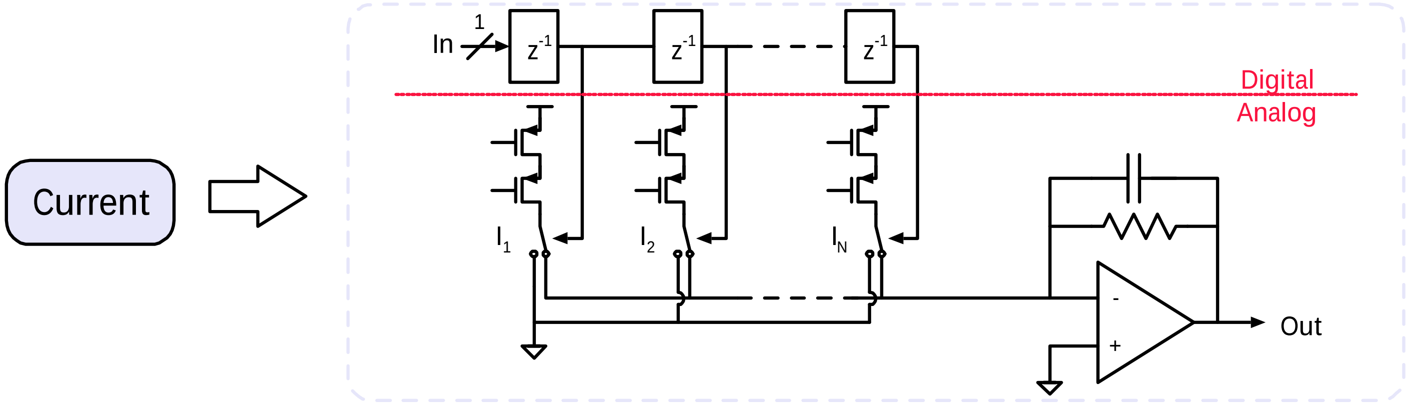
- Multi-bit output and high order modulation allows for low OSR
- Stable for 1st and 2nd order cascaded loops
- Single-bit DAC in the signal path
- Multi-bit DAC in the noise path
- Semi-digital FIR filter in the signal path is an option

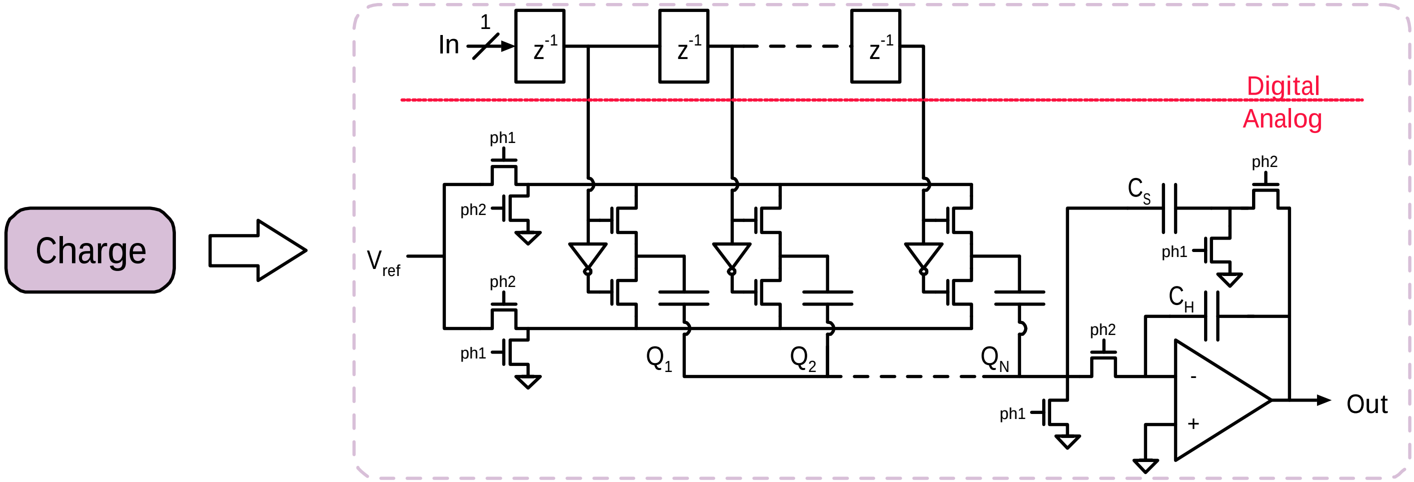
Semi-Digital FIR



- ❑ Semi-Digital FIRs can attenuate the large quantization noise generated at the output of single-bit DACs
- ❑ FIR coefficient mismatch will affect the filter response without introducing distortion → 1-bit DAC linearity preserved
- ❑ The stop band attenuation and number of taps is limited by the coefficient accuracy
- ❑ Phase linearity
- ❑ Requirements for subsequent reconstruction filters are relaxed

Semi-Digital FIR implementations

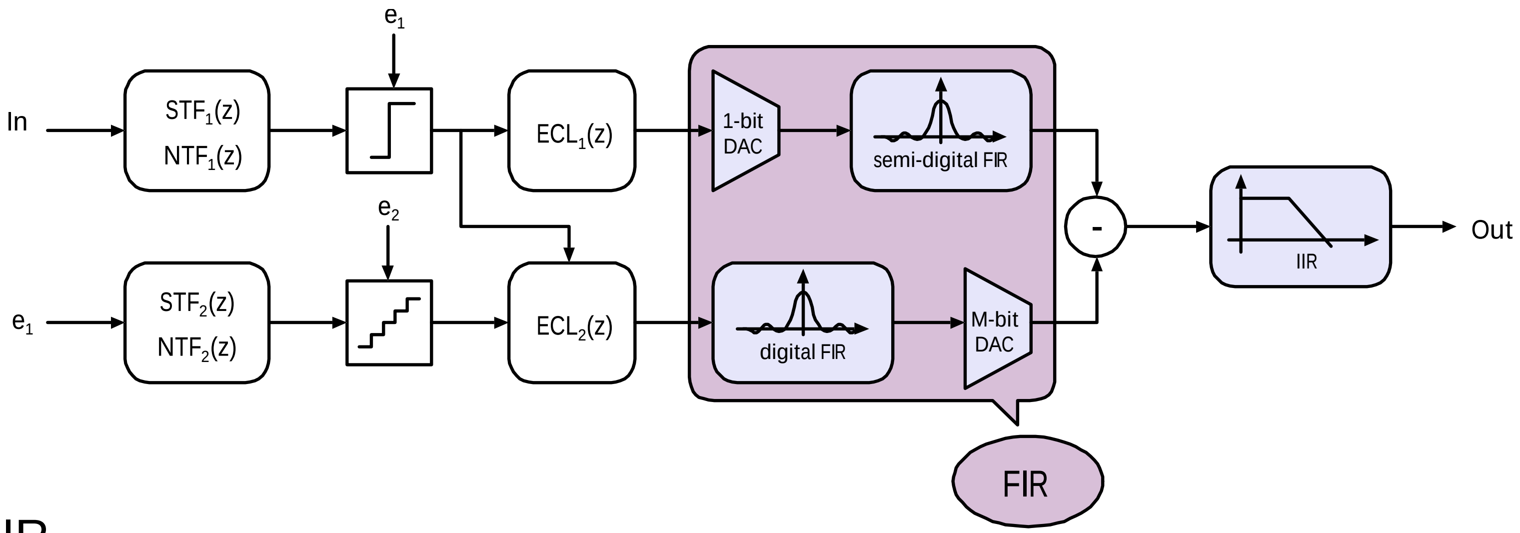




☺ For symmetrical FIR the shift register can be folded and minimum tap halved

❑ In the charge domain Direct Charge Transfer is an interesting alternative

Hybrid FIR/IIR Reconstruction Filter

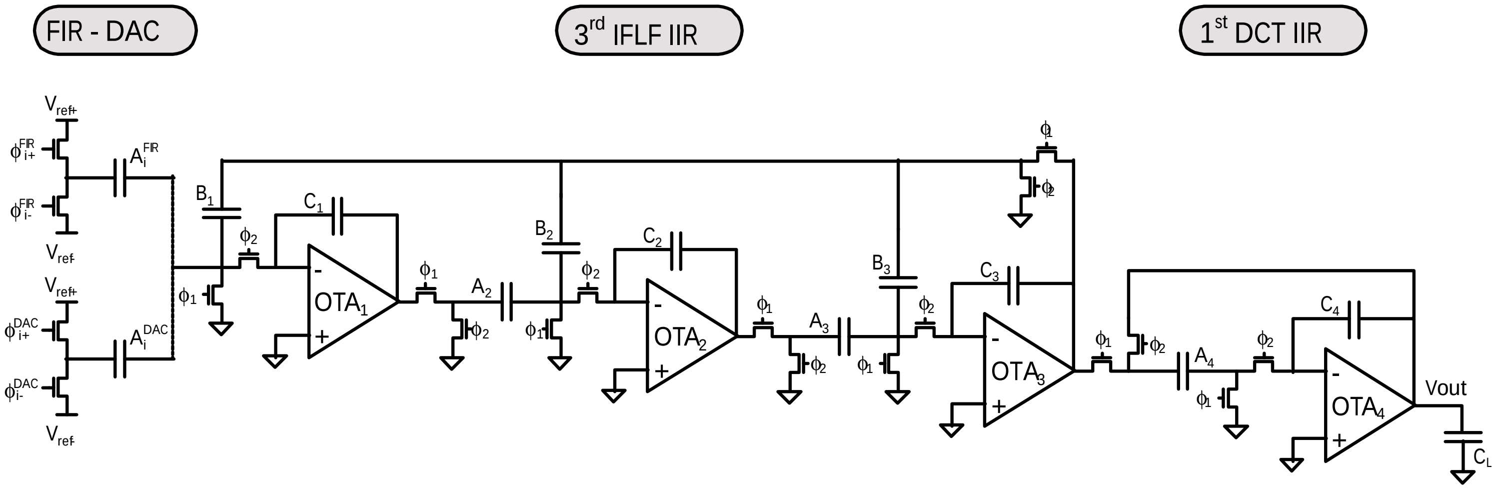


- ❑ FIR
  - Signal-path : single-bit DAC • semi-digital FIR
    - ✓ no signal distortion
  - Noise-path : digital FIR • multi-bit DAC
    - ✓ DAC nonlinearities and path mismatches affect “only” quantization noise cancellation
- ❑ IIR
  - Relaxed requirements after FIR filtering

❸

MADBRIC ΣΔ D/A Design Example

MADBRIC FIR-IIR implementation



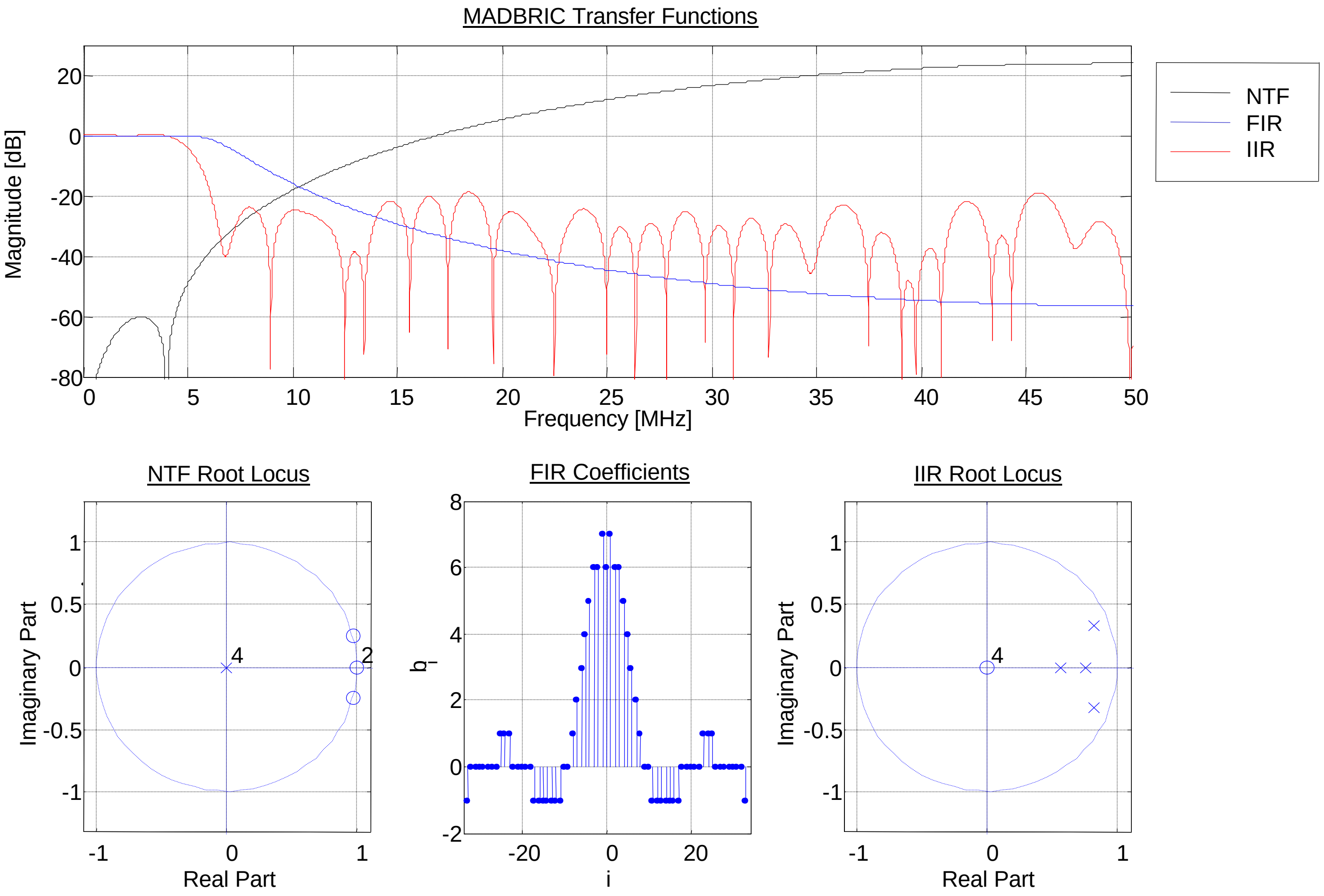
- FIR-DAC
  - 63 levels DAC
  - 67-tap FIR
- 4th order poles only IIR
  - 3rd order Inverted Follow the Leader Feedback
  - 1st order Direct Charge Transfer
- Fully differential
- Regulated folded cascode OTAs

Target Specifications	
Band	4MHz
Sampling freq.	100MHz
Vdd	1.8V
SNR in-band	86 dB
SNR full-spectrum	72 dB
Max in-band Ripple	0.5 dB
Max in-band Group Delay dev.	5% =1.25 samples

MADBRIC Transfer Functions

- ❑ Filter strategy
  - ▪ FIR attenuates close to the signal bandwidth
  - ▪ IIR has relaxed cut-off frequency requirement
  - ☺ Low in-band group delay deviation

- ❑ The entire design is defined by
  - ▪ NTF zeros
  - ▪ FIR taps
  - ▪ IIR poles

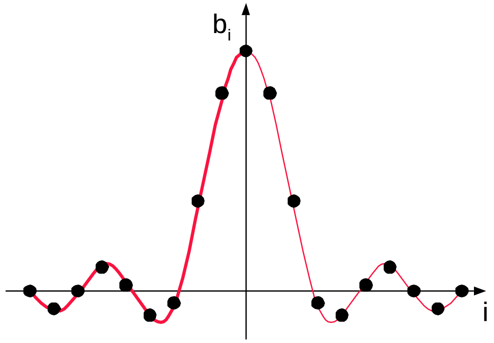


MADBRIC SC FIR Design Considerations

- FIR
  - Analog vs. Digital

    → Matching vs. Truncation
  - Multi-bit DAC nr. levels is fixed by
    - 2^{nd} ΣΔ loop quantizer
    - coefficient word length
    - digital FIR output truncation
  - Coefficient accuracy limits
    - max stop-band attenuation
    - FIR length
  - Null coefficients are ideal

    → sample Sinc zero crossing
  - Few power of two sample coefficient representation



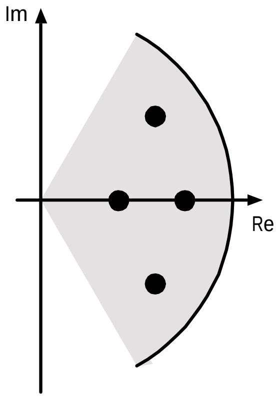
$$\text{Stopband Attenuation} \leq d_2 + \frac{\sqrt{p N}}{2} s_e$$

$d_2 =$ Ideal Stopband Attenuation

$N =$ FIR Length

$s_e =$ Coefficient Gaussian std

MADBRIC SC IIR Design Considerations (I)



- ☐ IIR optimal pole locations
  - Is a nonlinear optimization problem

PROBLEM

$$\min \int_0^{f_s/2} \left| h_{NTF}(f) \cdot h_{FIR}(f) \cdot h_{IIR}(f) \right|^2 df$$

CONSTRAINTS

$$h_{FIR}(f) \cdot h_{IIR}(f) \Big|_{Ripple} \leq \text{Specification}$$

$$h_{FIR}(f) \cdot h_{IIR}(f) \Big|_{GDdev} \leq \text{Specification}$$

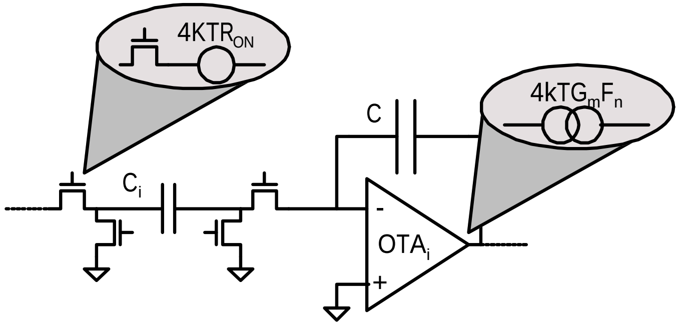
- ☐ Also the FIR coefficient could be ideally included in the optimization problem. This would be a more difficult mixed integer problem
- ☐ Transmission channel mask could be included

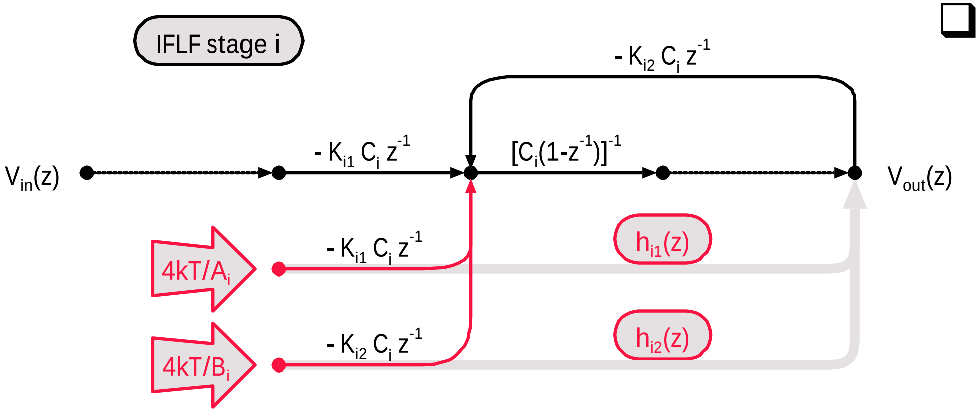
MADBRIC SC IIR Design Considerations (II)

- ❑ Thermal noise
  - Wideband CMOS switch and OTA noise is undersampled

    → noise folds into the signal band
  - Sampled noise decreases with C

    → optimal capacitance assignment maximize SNR



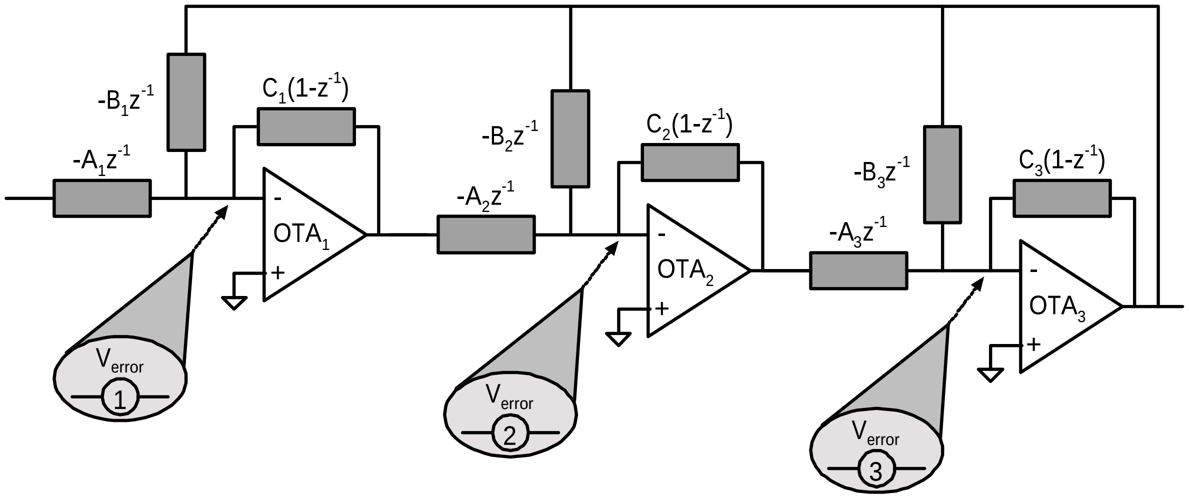


- ❑ Noise approximation for optimal assignment [Kaelin, TCAS, Nov.1991]

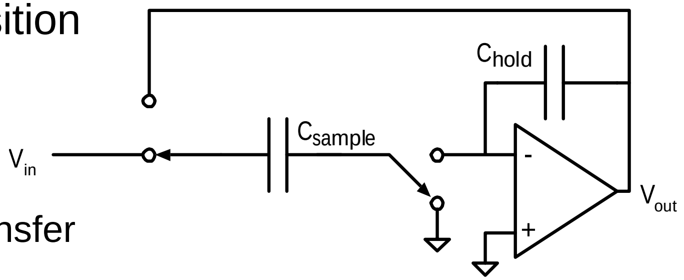
$$\int_0^\infty \sum_i \sum_j \frac{4kT}{K_{ij}} \cdot \left|h_{ij}(f)\right|^2 \cdot \frac{1}{C_i}\, df$$

MADBRIC SC IIR Design Considerations (III)

- ❑ 3rd IFLF SC filter
  - Noise shaping principle
    - The in-band KT/C noise, OTA noise dominated by the first stage
    - Offset and 1/f noise also dominated by first stage



- ❑ 1st DCT filter [Fujimori, JSSC,Dec.1998]
  - Good choice for sampled to continuous time transition
    - The output is passively generated without OTA assistance
    - OTA drives only the C_{sample} bottom plates
    - Wideband OTA noise in feedback during charge transfer phase is not undersampled → will not alias



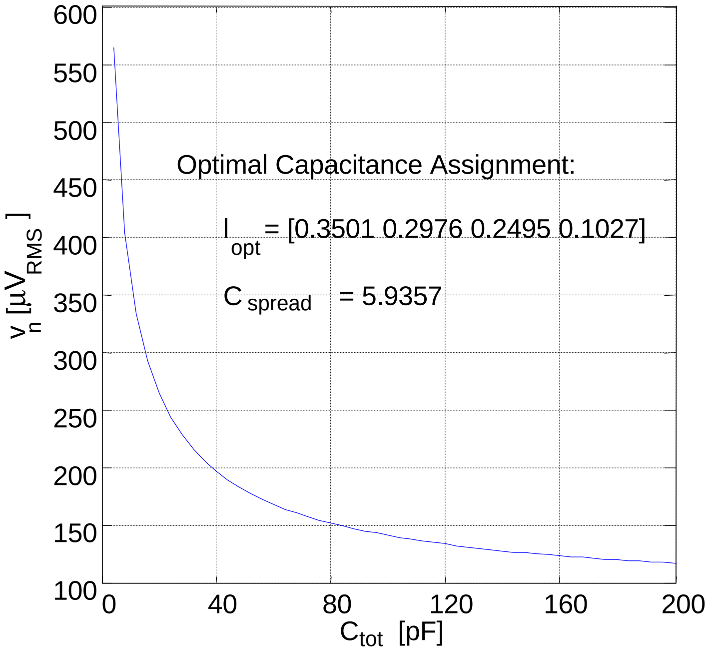
MADBRIC Optimal Capacitance Assignment

The total capacitance is distributed for optimal noise performance among all the integrator stages

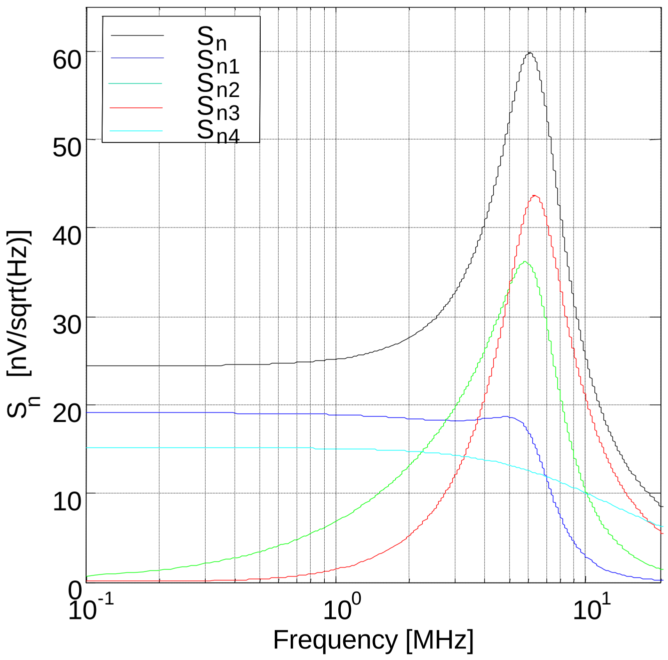
😐 In order to meet the full-spectrum SNR specification

C_{tot} > 100pF → Power > 120mW (with RFC OTAs)

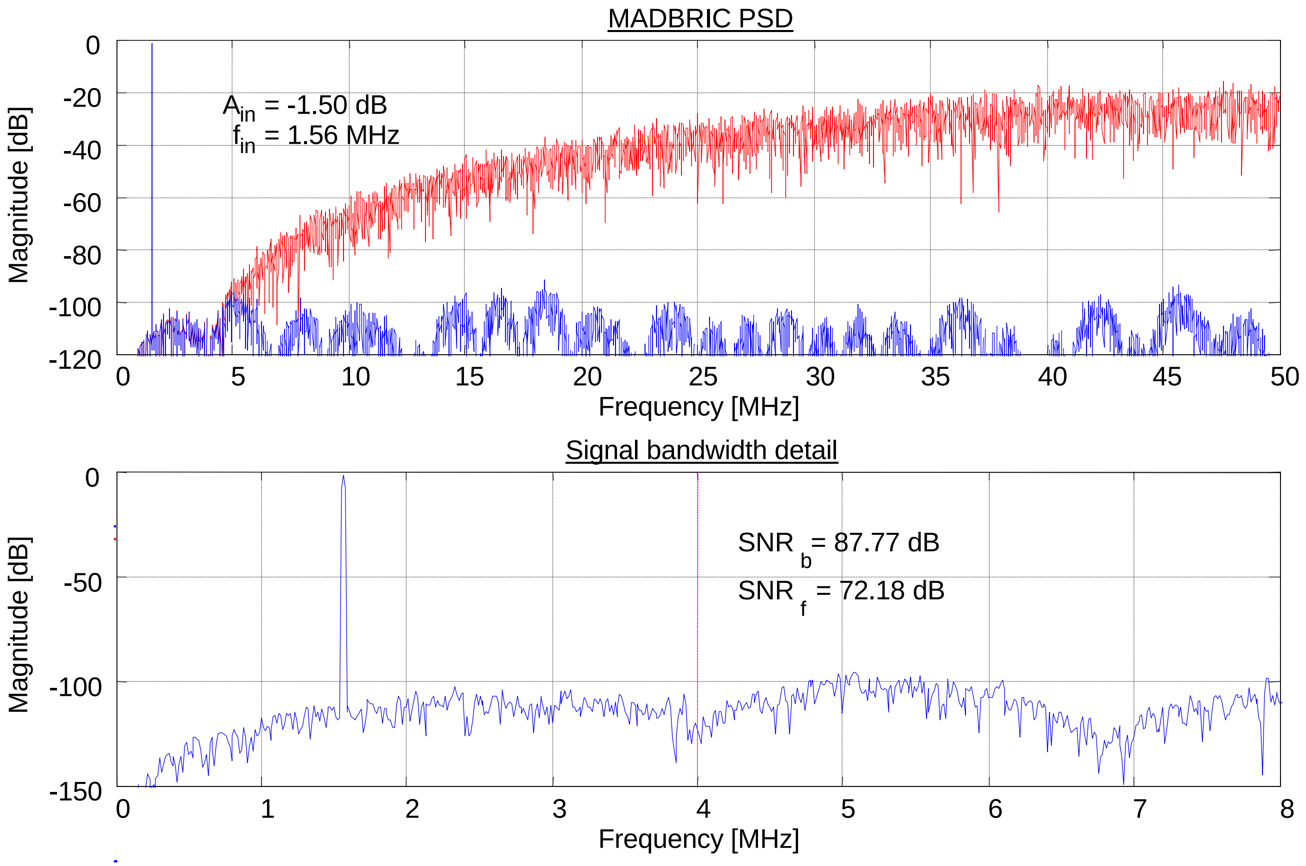
Total Output Noise vs. Total Capacitance



Output noise PSD (C_{tot} = 100pF)



Simulation Results: Matlab

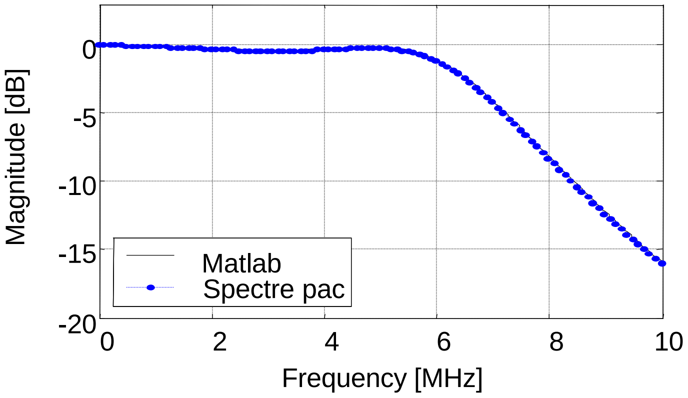


☹ Thermal noise and harmonic distortion reduce further the SNR.

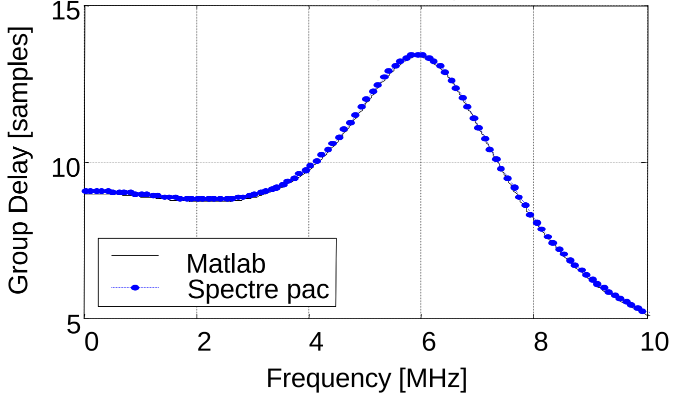
Simulation Results: Spectre Periodic Analysis

☺ Matlab and Spectre Periodic AC and noise analysis are in good agreement

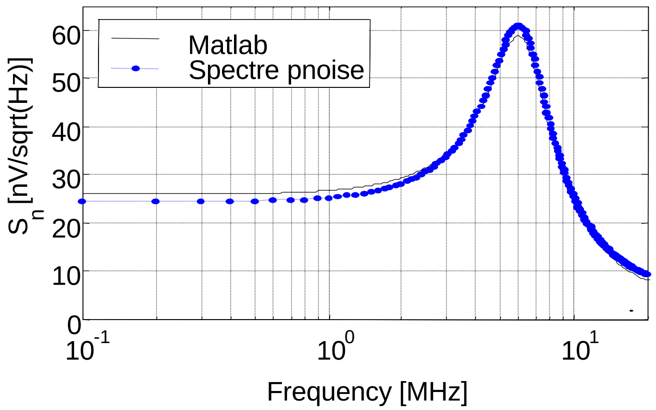
IIR Magnitude



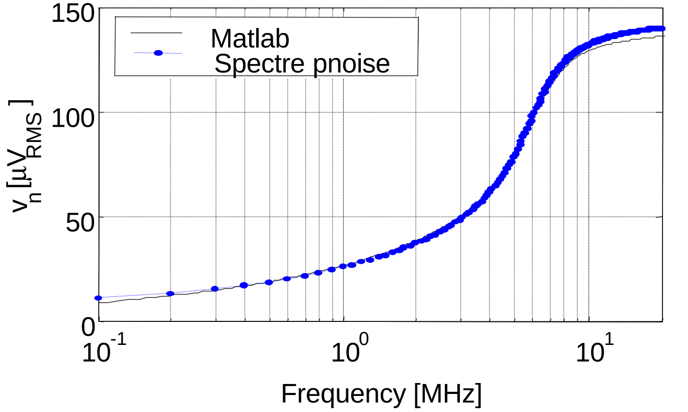
IIR Group Delay



IIR Output Noise PSD (C_{tot}=100pF)

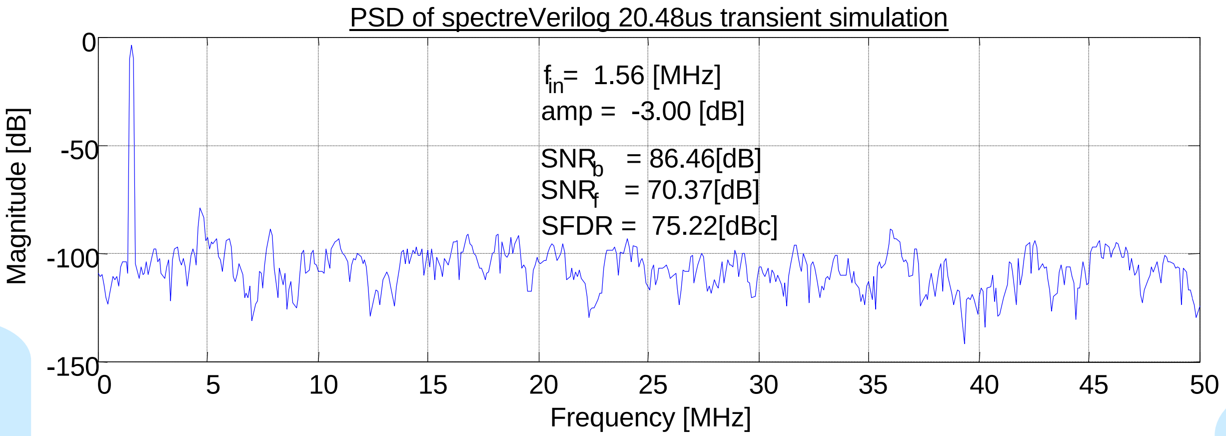


IIR Output Noise Cumulative PSD (C_{tot}=100pF)

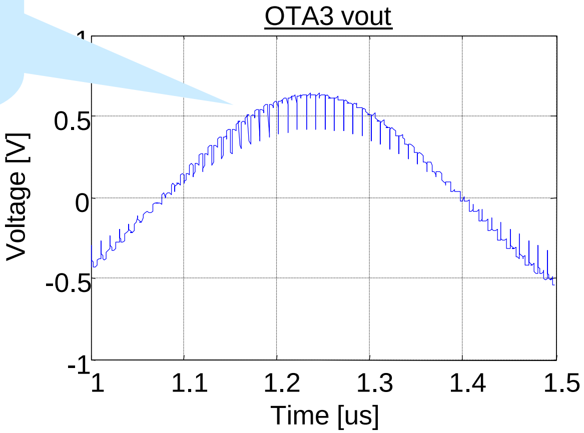


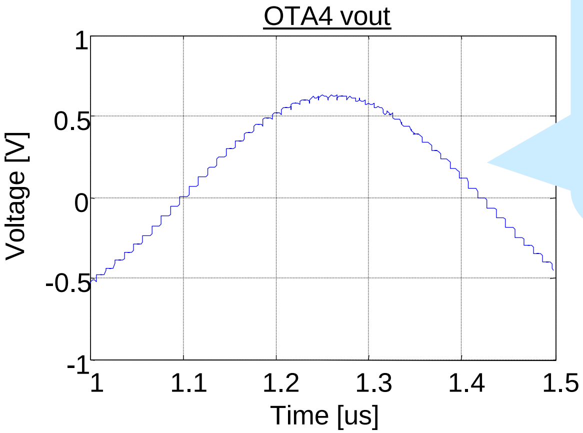
Simulation Results: spectreVerilog

- ☺ Matlab and spectreVerilog simulation are also in good agreement
- ❑ SFDR can be estimated with mixed-signal simulations in a reasonable amount of time



The output voltage from the IFLF SC filter needs only to settle to the right value





Any signal-dependent nonlinear settling in the DAC output will cause distortion when observed in continuous time

Summary

- ❑ DAC basic concept reviewed
- ❑ In ΣΔ DAC the reconstruction filter is the real design problem
- ❑ As yet, no DAC architecture of choice for xDSL applications
- ❑ For broadband application ΣΔ modulation can be used but with low OSR and multi-bit outputs
- ❑ MADBRIC design example and simulation results