

**High-Speed**  
**Folding and Interpolation**  
**A/D Converters**

Jürgen Hertle  
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# Outline

- General Features
- Architecture and Signal Shapes
- Limitations of Accuracy
- Techniques to Improve Accuracy
- Speed Considerations
- Noise Considerations
- Design Example

# General Features of Folding and Interpolating A/D Converters

- flash like architecture
- folding
- interpolation
- Nyquist sampling
- low latency
- accuracy depends on zero-crossings only

excellent conversion speed

less comparators

less preamplifiers



reduced area and power requirements

better use of technology

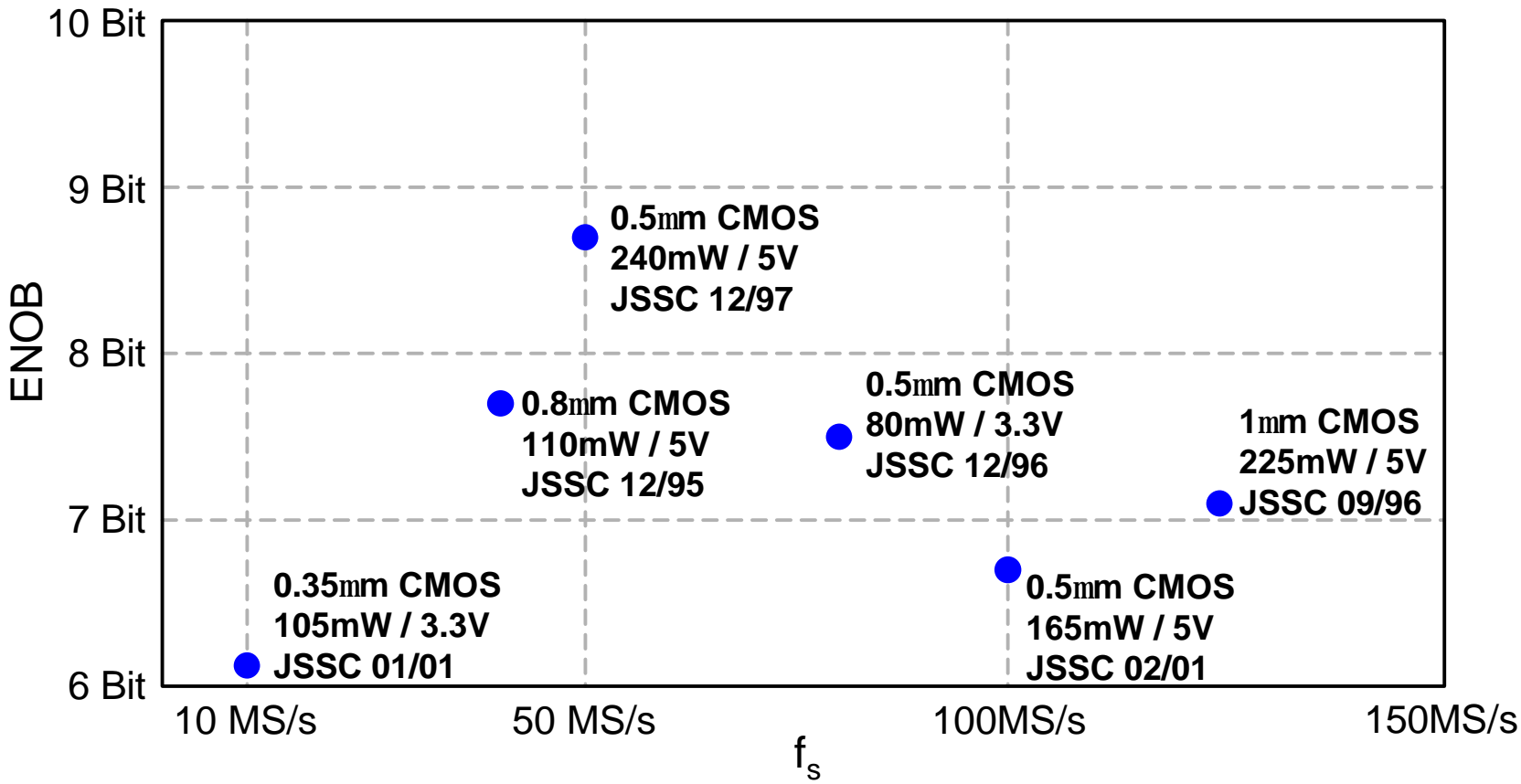
no oversampling

applicable in feedback loops

reduced linearity requirements

of internal blocks

# Published CMOS Folding and Interpolating ADCs

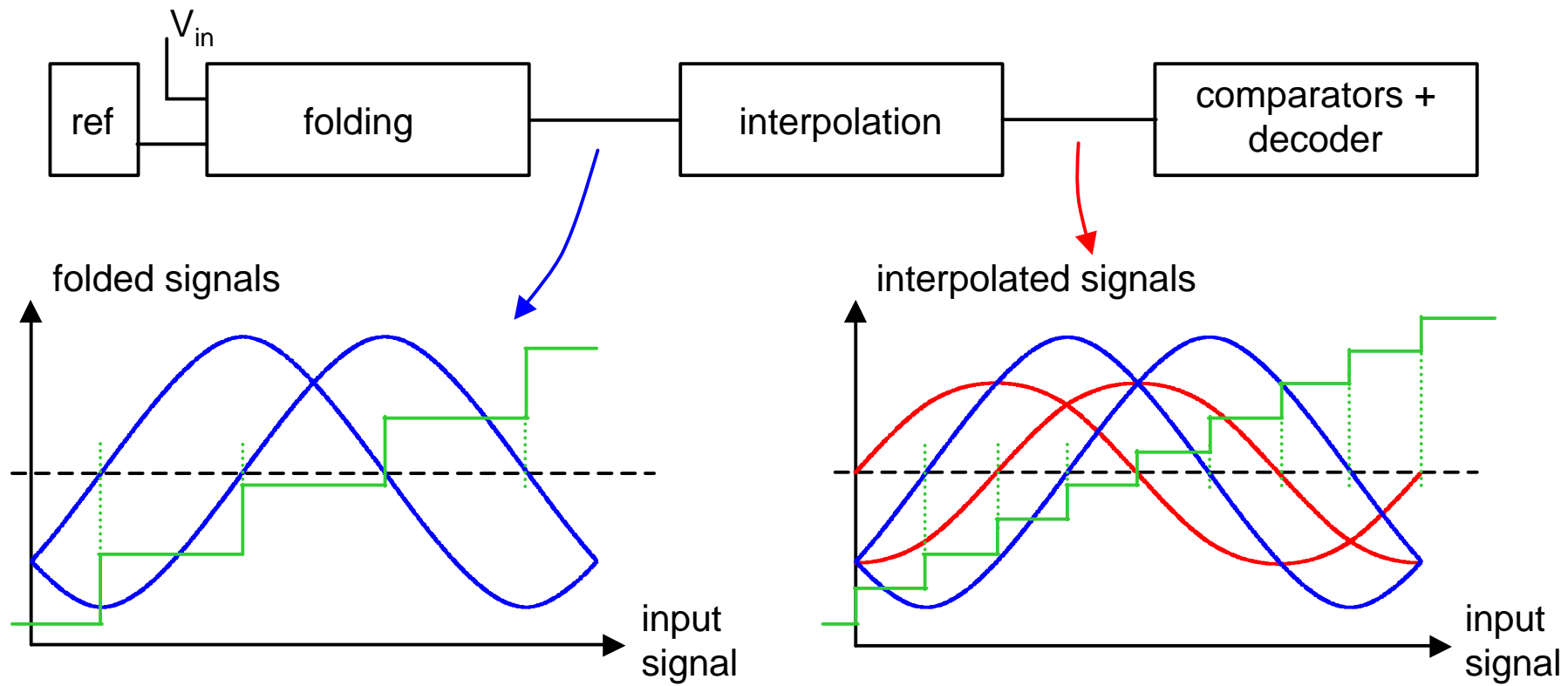


- currently limited to less than 10 Bit at 50-100 MS/s
- supply voltage > 3 V

only uncalibrated designs shown

# Signal Shapes in Folding and Interpolating ADCs

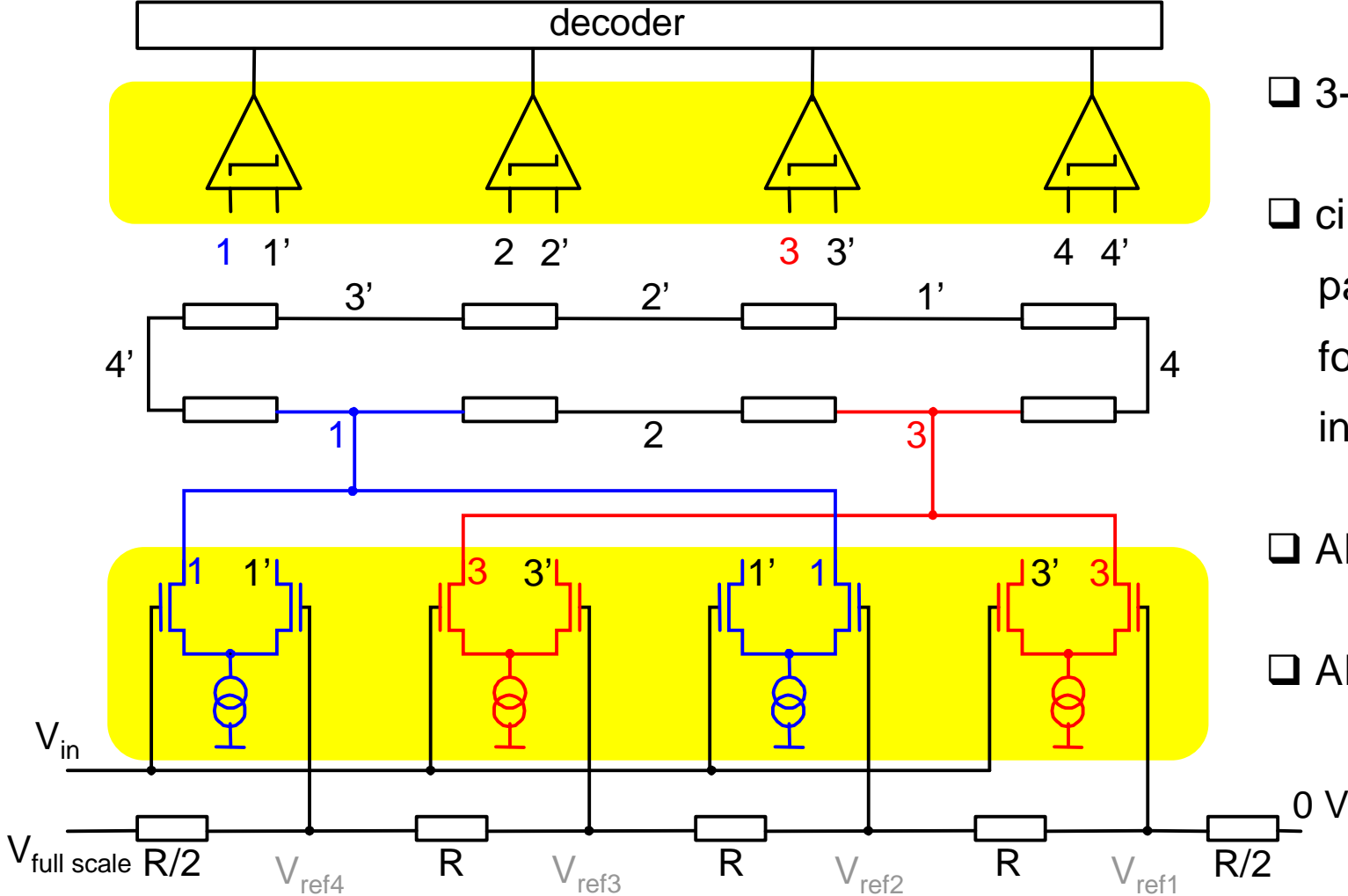
simplified block diagram



□ 2 parallel folding blocks with 2 folds

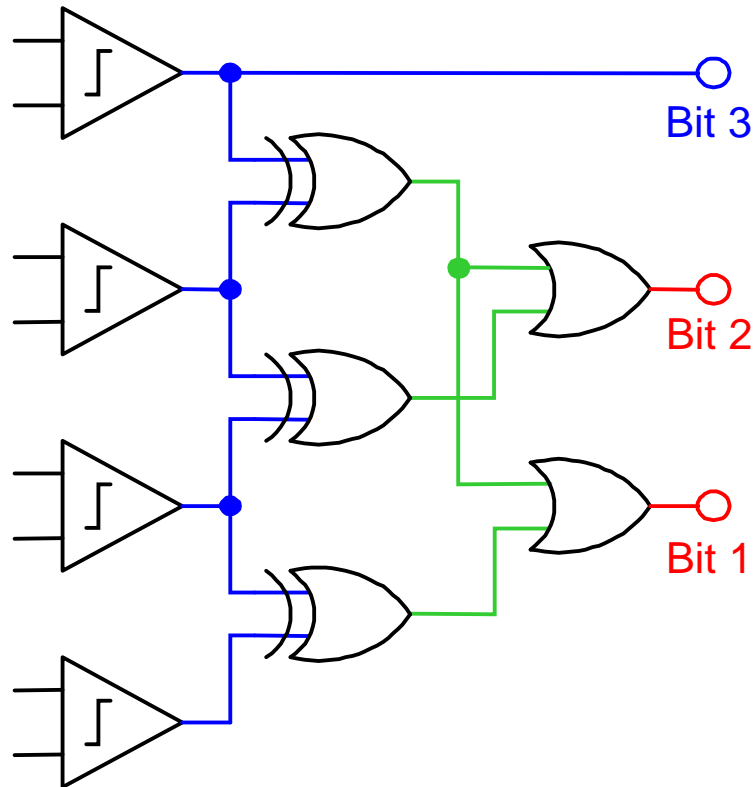
□ 2 times interpolation

# Converter Architecture on Device Level

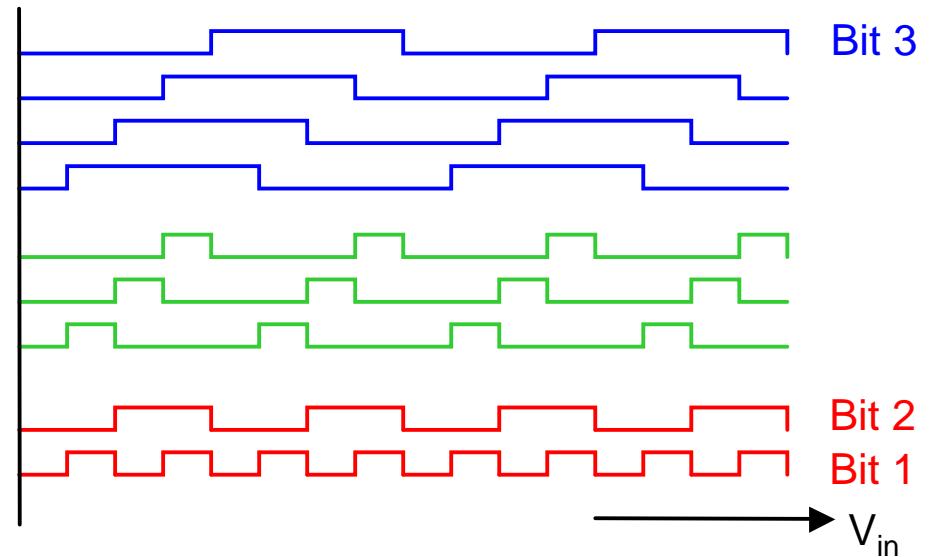


- 3-Bit converter
- circuit parameters:  
parallel folders:  $A=2$   
folding factor:  $F=2$   
interpolation factor:  $I=2$
- AF preamplifiers
- AI comparators

# Decoding



can be easily extended to correct bubbles in output code



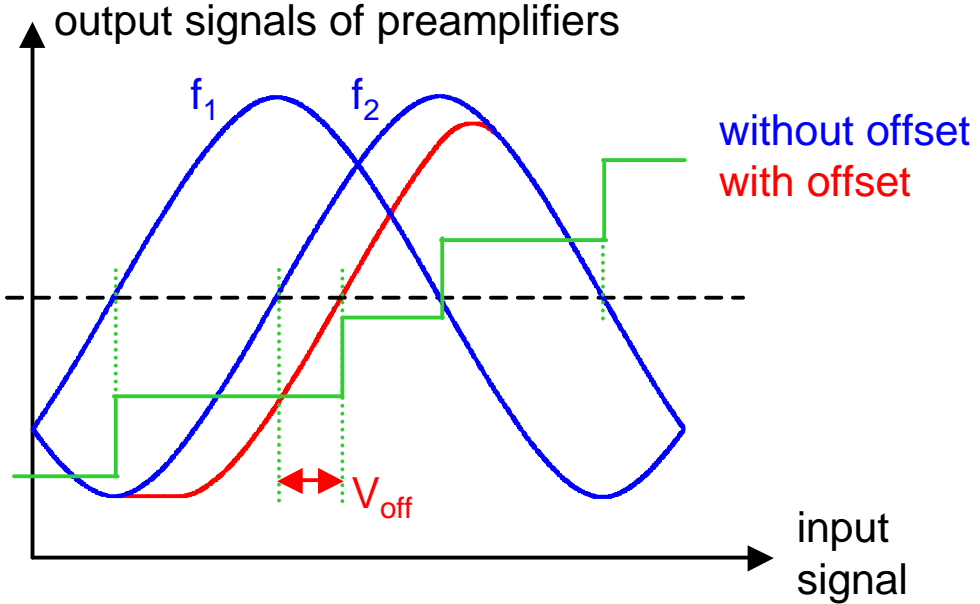
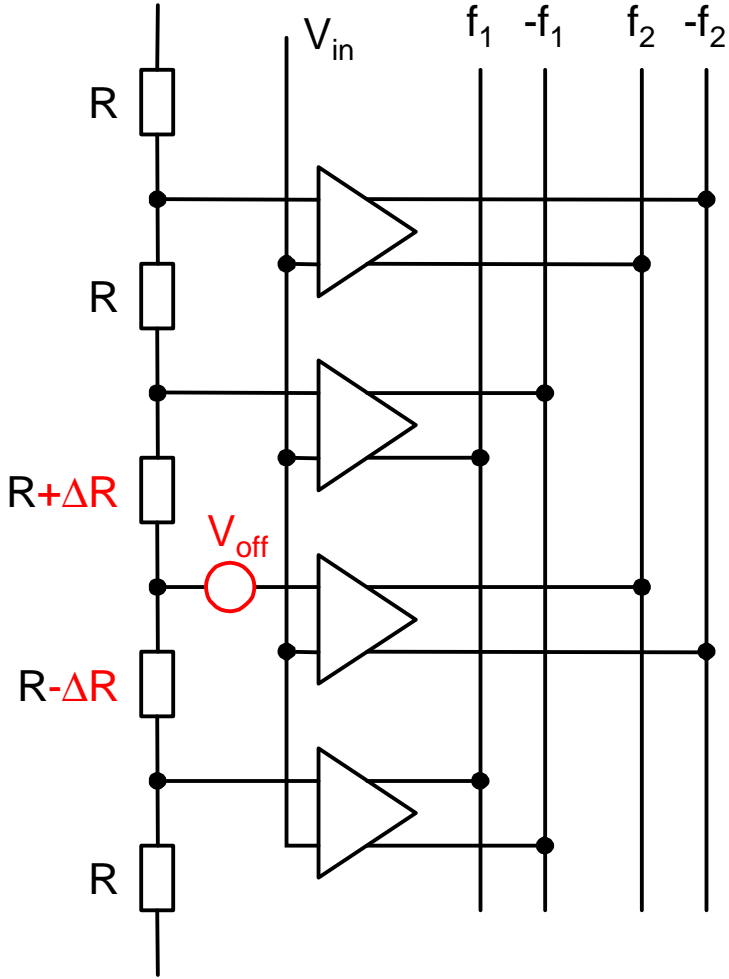
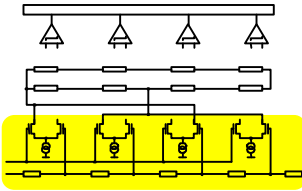
allocation of cyclic thermometer code to binary code

0000	000
0001	001
0011	010
0111	011
1111	100
1110	101
1100	110
1000	111

CTC contains one bit more of information than standard thermometer code

# Limitations of Zero-Crossing Accuracy (I)

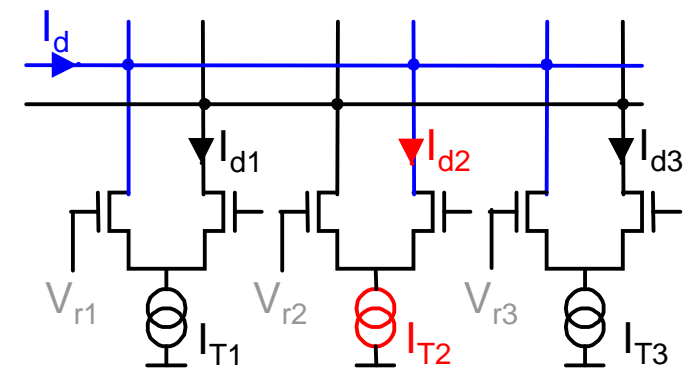
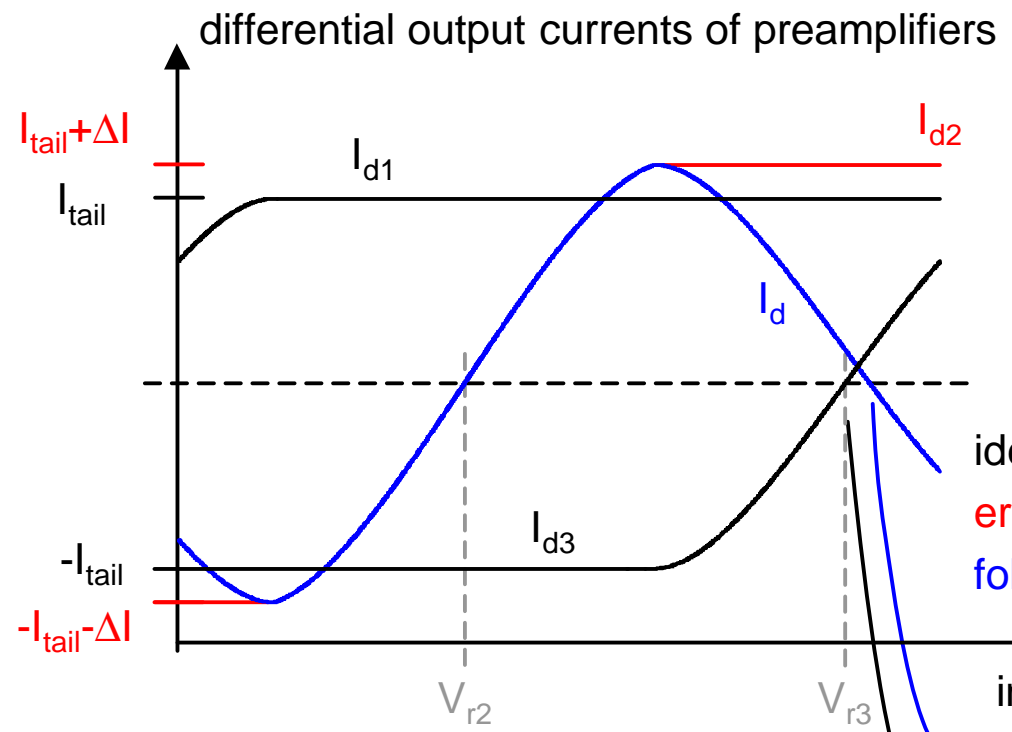
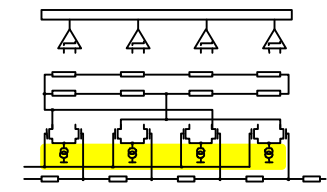
reference ladder and preamplifier offset



- ❑ translates directly into INL
- ❑ deteriorates DNL

# Limitations of Zero-Crossing Accuracy (II)

tail current mismatch of preamplifiers

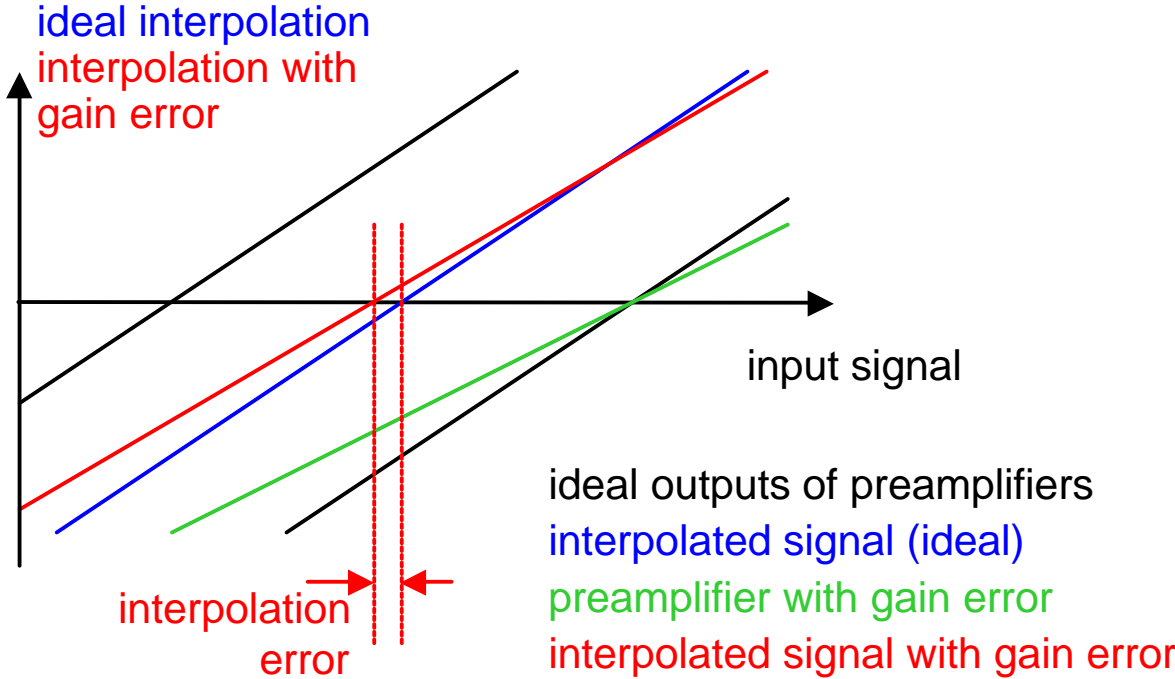
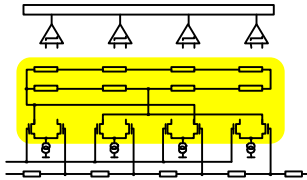


- ❑ affects INL
- ❑ deteriorates DNL

ideal tail current  
 erroneous tail current  
 folded signal ( $I_d = -I_{d1} + I_{d2} - I_{d3}$ )  
 input signal  
 zero-crossing due to mismatch  
 ideal zero-crossing

# Limitations of Zero-Crossing Accuracy (III)

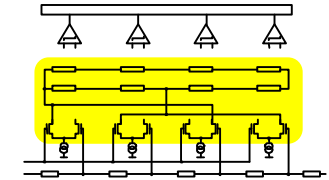
gain mismatch of preamplifiers



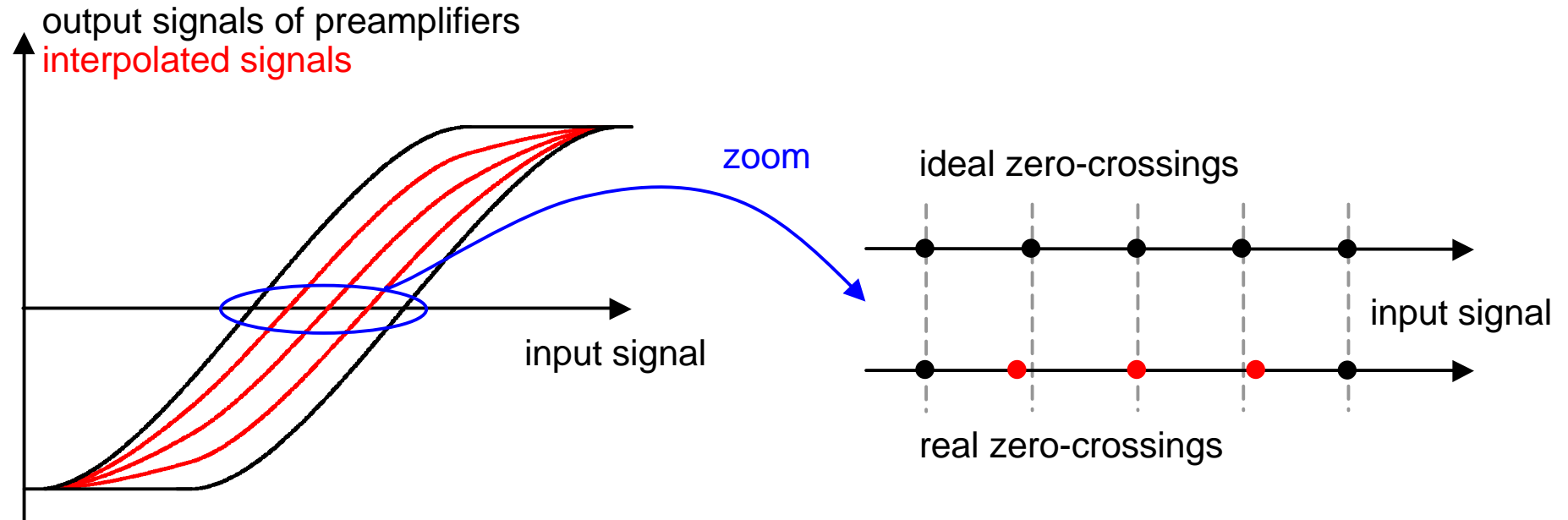
- zero-crossings of non interpolated signals not affected
- zero-crossing of interpolated signal is altered

- increases INL
- deteriorates DNL

# Limitations of Zero-Crossing Accuracy (IV)



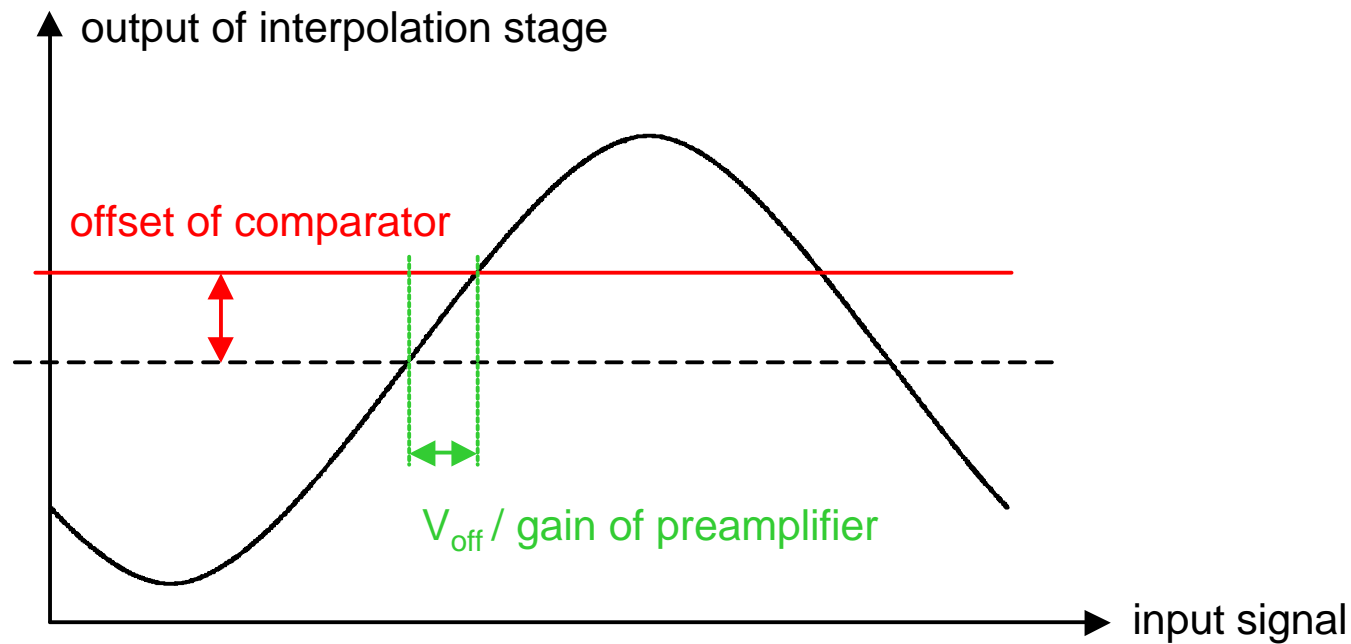
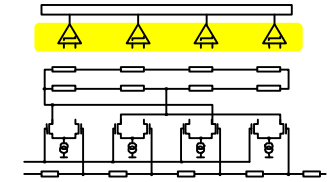
nonlinearity of preamplifiers



- ❑ nonlinearity of preamplifiers prevents perfectly linear interpolation
- ❑ no error for interpolation of 2 (perfect resistor matching assumed)

# Limitations of Zero-Crossing Accuracy (V)

offset voltage of comparators



- increases INL
- dominates DNL

# Required Matching Parameters

for  $\text{INL} < 1 \text{ LSB}$

$\text{NOB} = \text{Number of Bits}$

- ❑ preamplifier offset

$$V_{\text{offset preamplifier}} < \frac{V_{\text{full scale}}}{2^{\text{NOB}}}$$

- ❑ resistor ladder matching

$$\frac{\Delta R}{R} < \frac{1}{2^{\text{NOB}}}$$

- ❑ tail current matching

$$\frac{\Delta I_T}{g_{m \text{ preamplifier}}} < \frac{V_{\text{full scale}}}{2^{\text{NOB}}}$$

- ❑ comparator offsets

gain-bandwidth trade-off

$$V_{\text{offset comparator}} < \frac{V_{\text{full scale}}}{2^{\text{NOB}}} \cdot \text{Gain}_{\text{preamplifier}}$$

# Design Techniques to Improve Accuracy (I)

increase transistor size for better matching

standard deviation of offset voltage:  $\sigma_{V_{\text{off}}} = \frac{A_{VT}}{\sqrt{WL}}$

example:  $V_{\text{full scale}} = 2 \text{ V}$

1 LSB = 2 mV (10-Bit accuracy)

$A_{VT} = 8..10 \text{ mV } \mu\text{m}$  (typical for 0.25  $\mu\text{m}$  technology)

$$\frac{10\text{mV } \mu\text{m}}{\sqrt{WL}} < \frac{2\text{mV}}{3} \Rightarrow WL = 225\mu\text{m}^2$$

far too big to get reasonable speed

# Design Techniques to Improve Accuracy (II)

## calibration of offsets

- ❑ autozero
  - reduces available settling time
  - power hungry
  
- ❑ background calibration
  - synchronization of calibration and normal operation critical
  - difficult to route

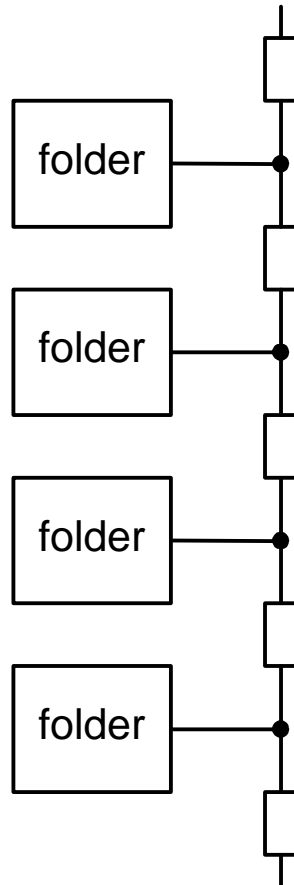
general problem:

switching signals near their Nyquist frequency very problematic due to

- charging errors
- harmonic distortion

# Design Techniques to Improve Accuracy (III)

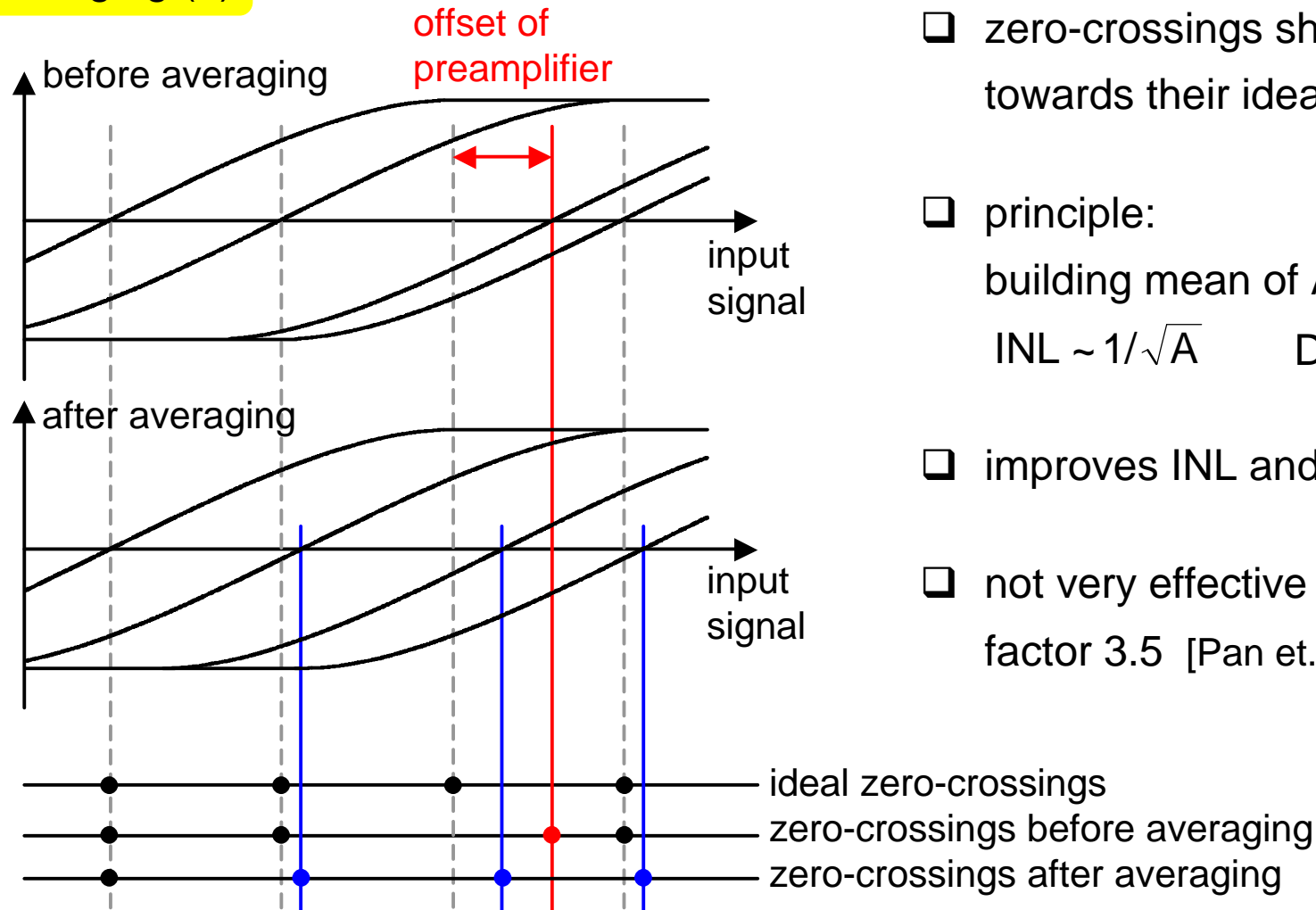
## averaging (I)



- ❑ insert lateral resistors between outputs of folders
- ❑ make outputs depend on each other
- ❑ averages offsets of preamplifiers which are near signal level
- ❑ effective increase of input transistor area

# Design Techniques to Improve Accuracy (IV)

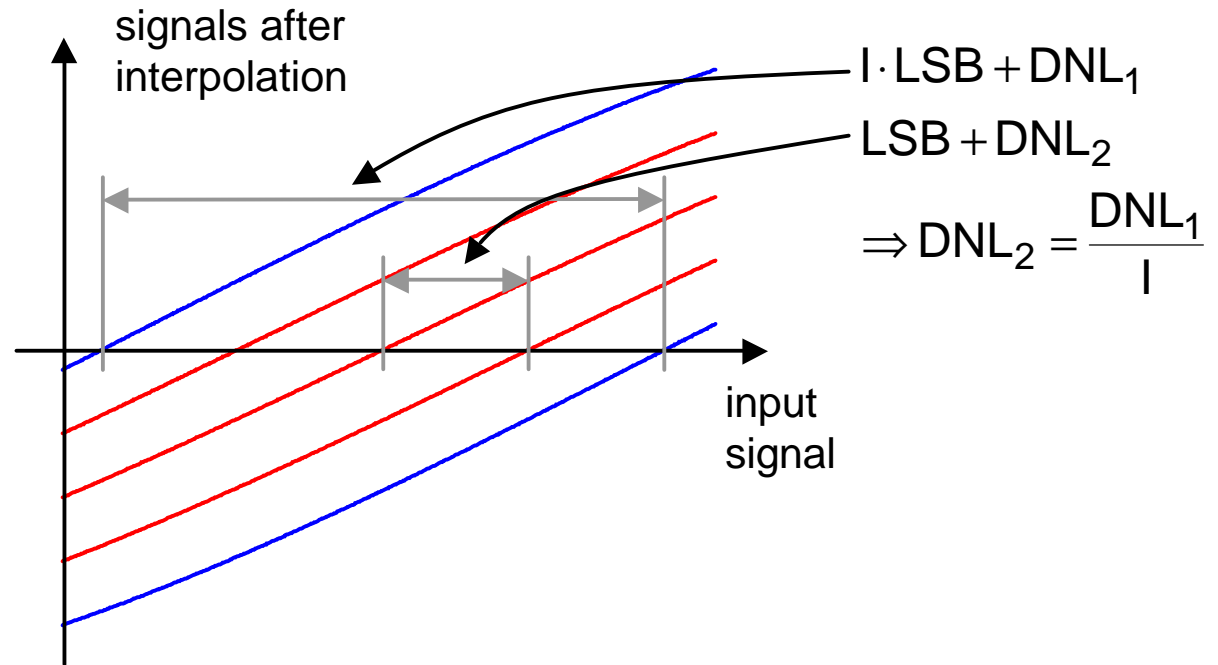
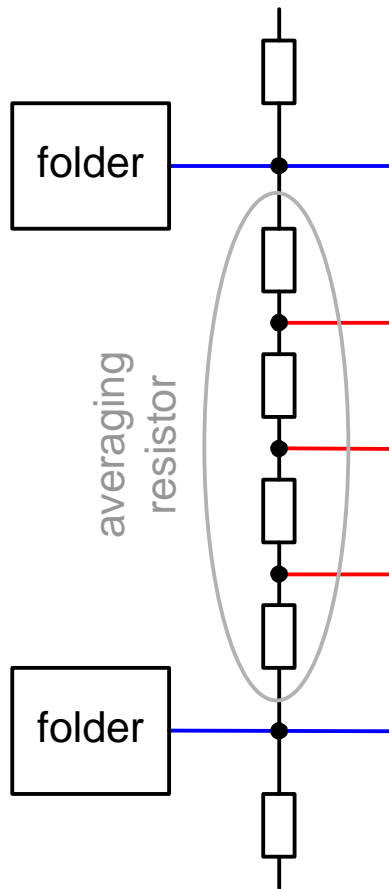
## averaging (II)



- ❑ zero-crossings shifted towards their ideal position
- ❑ principle:  
building mean of  $A$  active signals  
 $INL \sim 1/\sqrt{A}$      $DNL \sim 1/A$
- ❑ improves INL and DNL
- ❑ not very effective  
factor 3.5 [Pan et.al., ISSCC 2000]

# Design Techniques to Improve Accuracy (V)

interpolation



- ❑ DNL improved by interpolation factor  $I$ 
  - valid for all stages before interpolation
  - **NOT** valid for comparators
- ❑ INL remains unaffected

# Design Techniques to Improve Accuracy (VI)

## tail currents of preamplifiers

- use very big transistors (current source at no speed limiting node)
- use current sources with high output resistance (cascode, regulated casode)
- apply techniques known from D/A Design

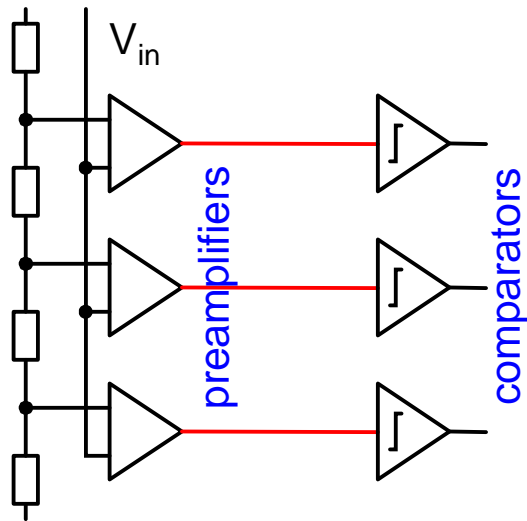
## offset voltages of comparators

- increase gain in preceding stages
- ⚡ gain must be within some bounds to guarantee proper interpolation

# Conversion Rate (I)

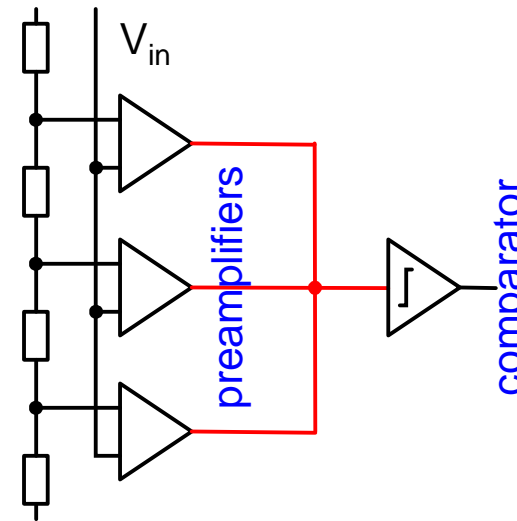
comparison between flash and folding architecture

flash quantizer



$$f_{3dB} = \frac{1}{2\pi R(C_{\text{preamplifier}} + C_{\text{comparator}})}$$

folding quantizer



speed  
limiting  
node

$$f_{3dB} = \frac{1}{2\pi R(F \cdot C_{\text{preamplifier}} + C_{\text{comparator}})}$$

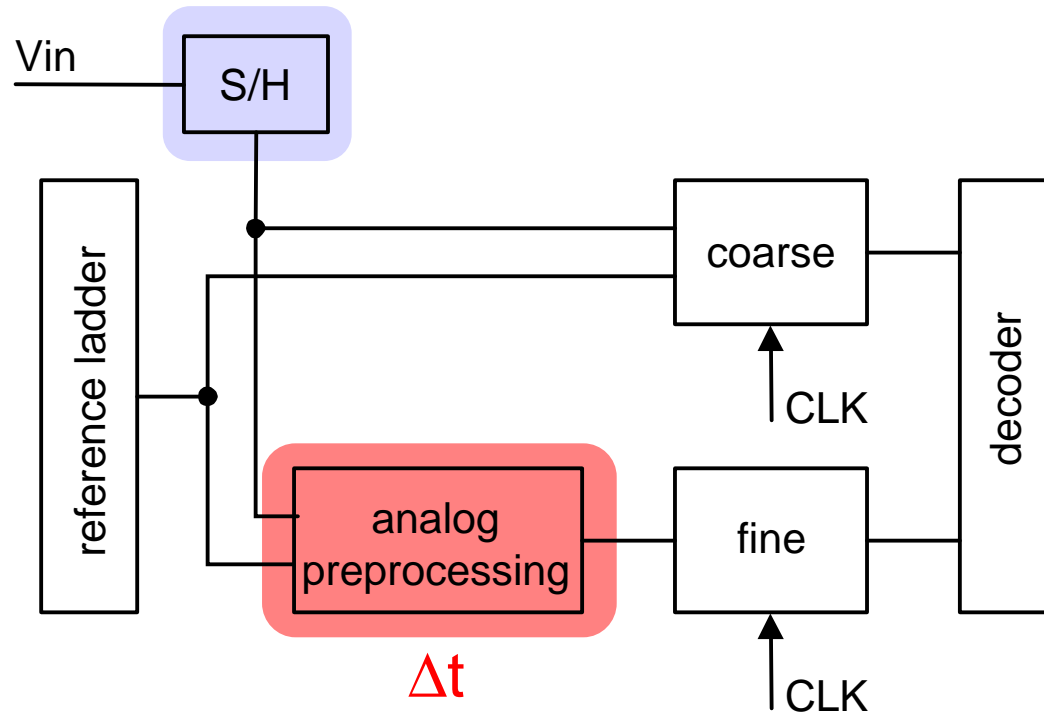
assume identical preamplifiers and comparators

bandwidth in folding architecture approximately reduced by folding factor F

internal signal frequency is **NOT** increased

# Conversion Rate (II)

benefit of sample and hold stage



$\Delta t$ : delay in analog preprocessing

- without sample/hold
  - $\Delta t$  can be modelled as jitter
  - $\Rightarrow$  very good delay matching between coarse and fine quantization necessary
- with sample/hold
  - no timing problem due to different propagation delays in coarse and fine quantization

# Noise Performance

## thermal noise

### □ dominant noise sources

- resistor ladder
- preamplifiers

### □ equivalent noise resistance

$$V_{\text{noise}} = \sqrt{4kT \cdot R_{\text{eq}} \cdot \text{Bandwidth}} < \frac{1}{3} \cdot \frac{1}{2} \text{LSB} = \frac{1}{3} \cdot \frac{V_{\text{FS}}}{2 \cdot 2^{\text{NOB}}}$$

$$R_{\text{eq}} < \left( \frac{1}{3} \cdot \frac{V_{\text{FS}}}{2 \cdot 2^{\text{NOB}}} \right)^2 \cdot \frac{1}{4kT} \cdot \frac{1}{\text{Bandwidth}}$$

### □ example: $V_{\text{FS}} = 2 \text{ V}$

NOB = 10 Bit

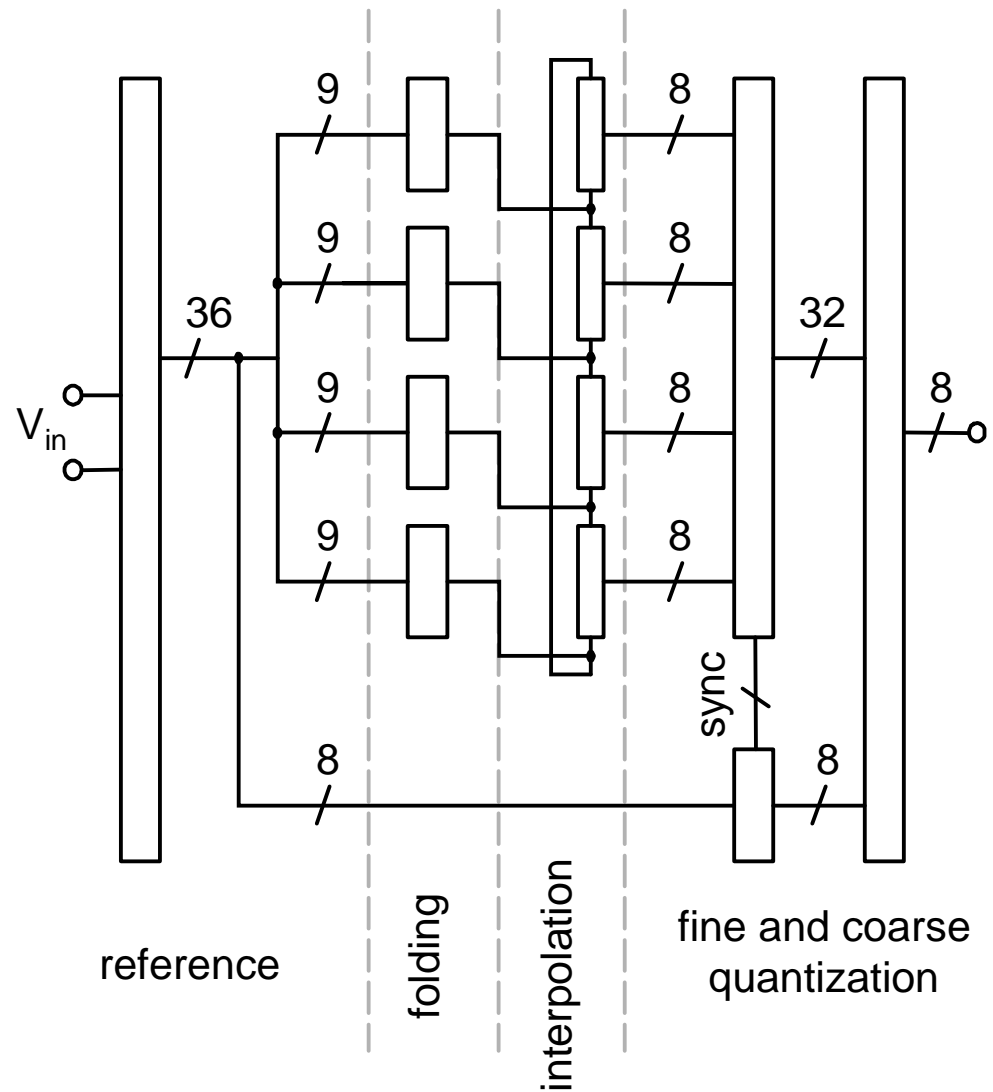
Bandwidth = 100 MHz

$$R_{\text{eq}} < 63 \text{ k}\Omega$$

noise is of minor importance as long as  $f_s < 200 \text{ MS/s}$  and NOB < 10 Bit

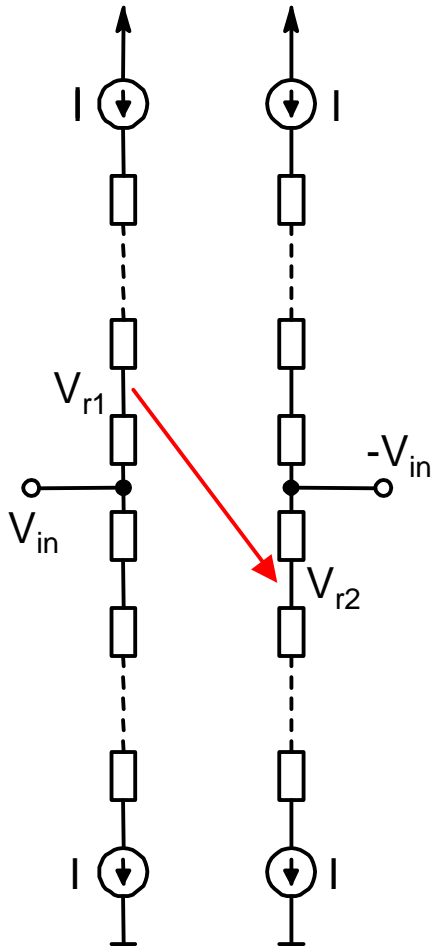
# Block Diagram of a 2.5-V 8-Bit 50-MS/s A/D Converter

- ❑ fully differential analog signal path
- ❑ overflow and underflow detection (combined with coarse quantization)
- ❑ 4 parallel folding blocks
- ❑ folding factor 8
- ❑ 9 cross-coupled preamplifiers for proper termination at ends of  $V_{FS}$
- ❑ 8 times interpolation
- ❑ 36 preamplifiers
- ❑ 40 comparators
- ❑ **optimized for low power consumption**



# Implementation Details

## reference ladder



- ❑ only one amplifier per level
- ❑ still fully differential
- ❑ reduced full scale by factor 2

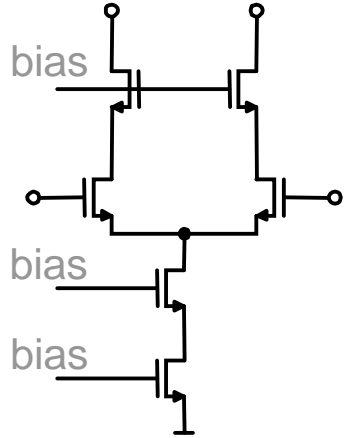
$$V_{r1} = V_{in} + R \cdot I$$

$$V_{r2} = -V_{in} - R \cdot I$$

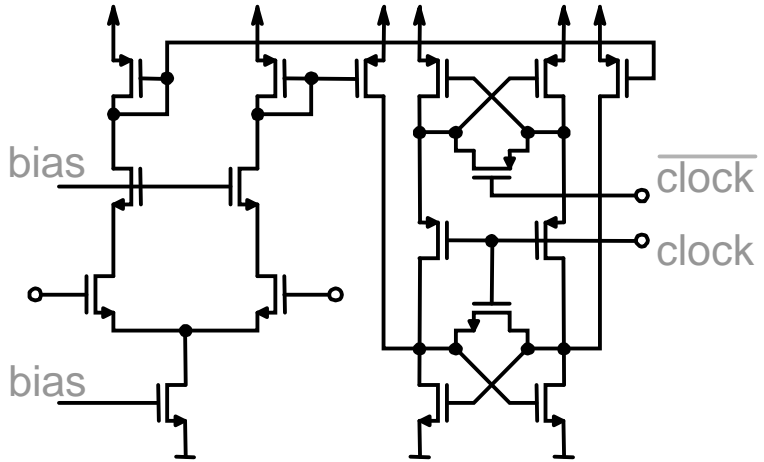
$$V_r = V_{r1} - V_{r2} = 2 \cdot (V_{in} + R \cdot I)$$

## preamplifier

- ❑ cascoded current source
- ❑ cascoded output to reduce  $C_{out}$  and  $C_{in}$



## comparator



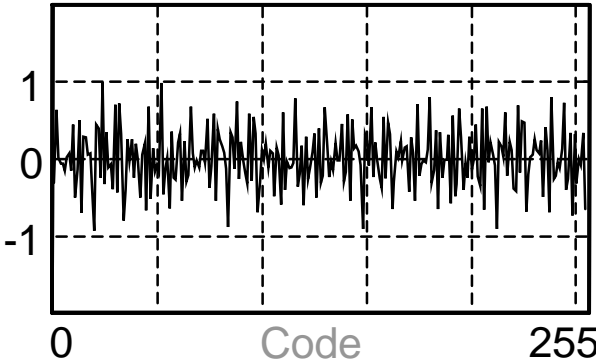
# Measurement Results

Chip Micrograph

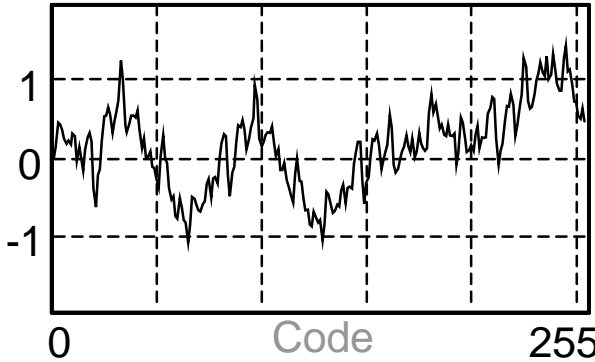


Technology: 0.25  $\mu\text{m}$  CMOS  
Chip Area: 2.4 mm<sup>2</sup>  
Power Consumption: 50 mW

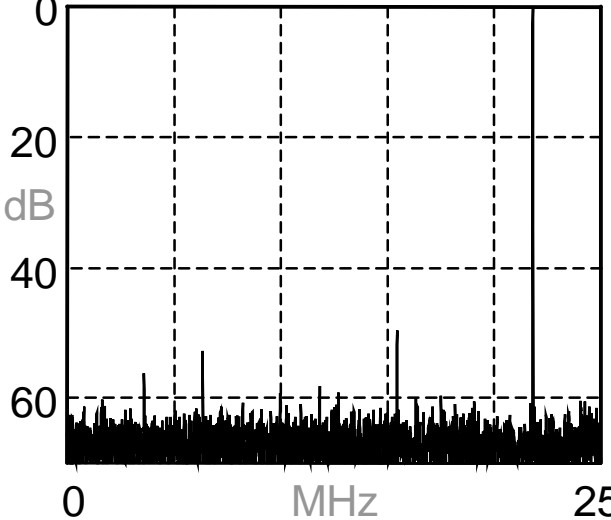
DNL in LSB



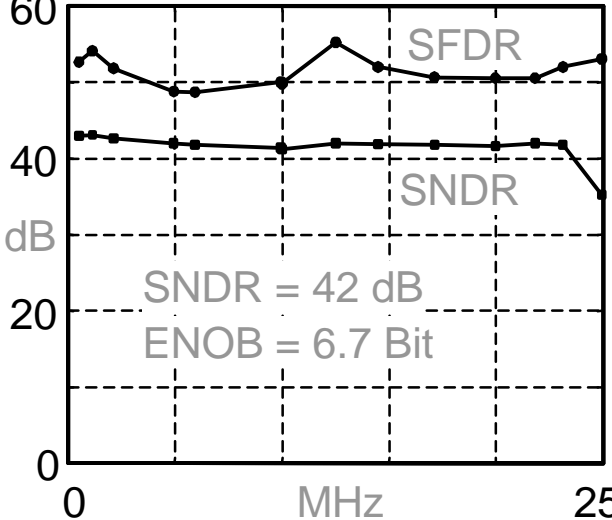
INL in LSB



Spectrum at 21.8 MHz



SNDR and SFDR



# Summary

- ❑ general features of folding and interpolating ADCs
  - application areas compared to pipelined ADC and  $\Sigma\Delta$  ADC
- ❑ limitations of accuracy
  - mismatch in reference ladder (INL)
  - offset of preamplifiers (INL)
  - tailcurrent mismatch (INL)
  - offset of comparators (INL + DNL)
- ❑ techniques to improve accuracy
  - averaging (INL and DNL)
  - interpolation (DNL)
- ❑ conversion rate and noise aspects briefly discussed
- ❑ design and measurement results of 8-Bit 50-MS/s ADC