

# **Pipelined A/D Converters for Telecommunication Applications**

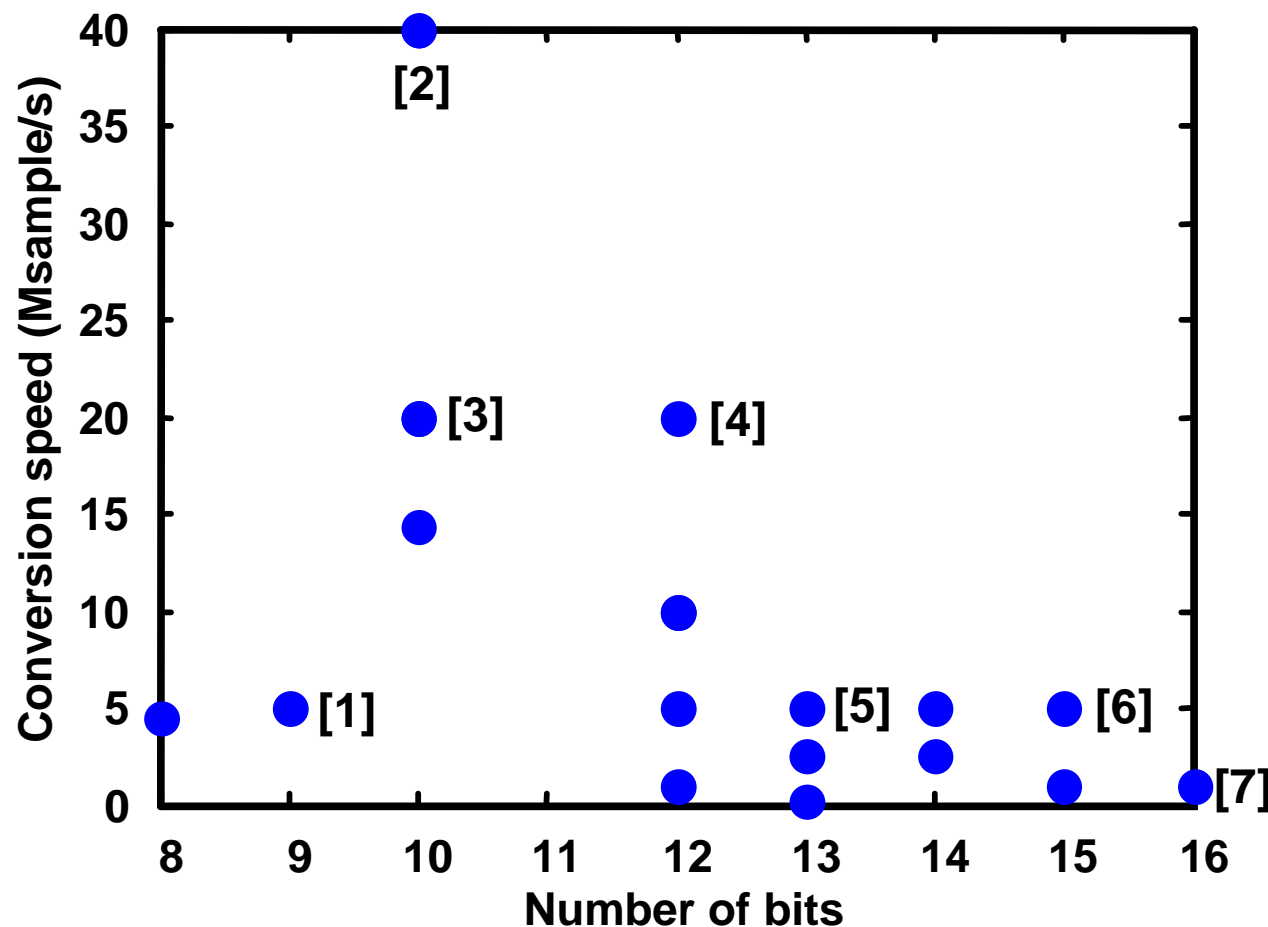
Dr. Clemens Hammerschmied

October 22<sup>nd</sup>, 2001

# Outline

- ❑ Achievable specifications
- ❑ Building blocks
- ❑ Accuracy
- ❑ Speed
- ❑ Noise
- ❑ Design example

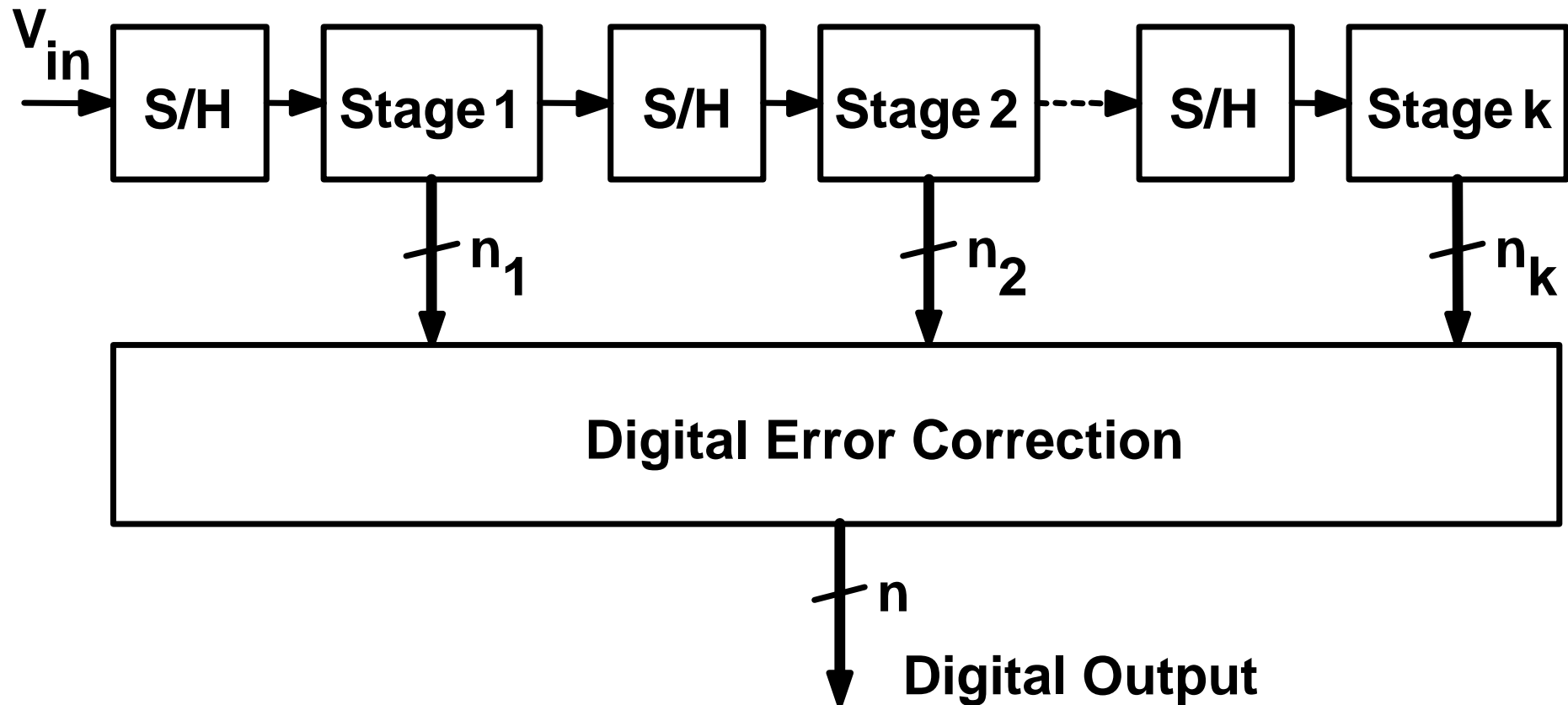
# Published Pipelined A/D Converters



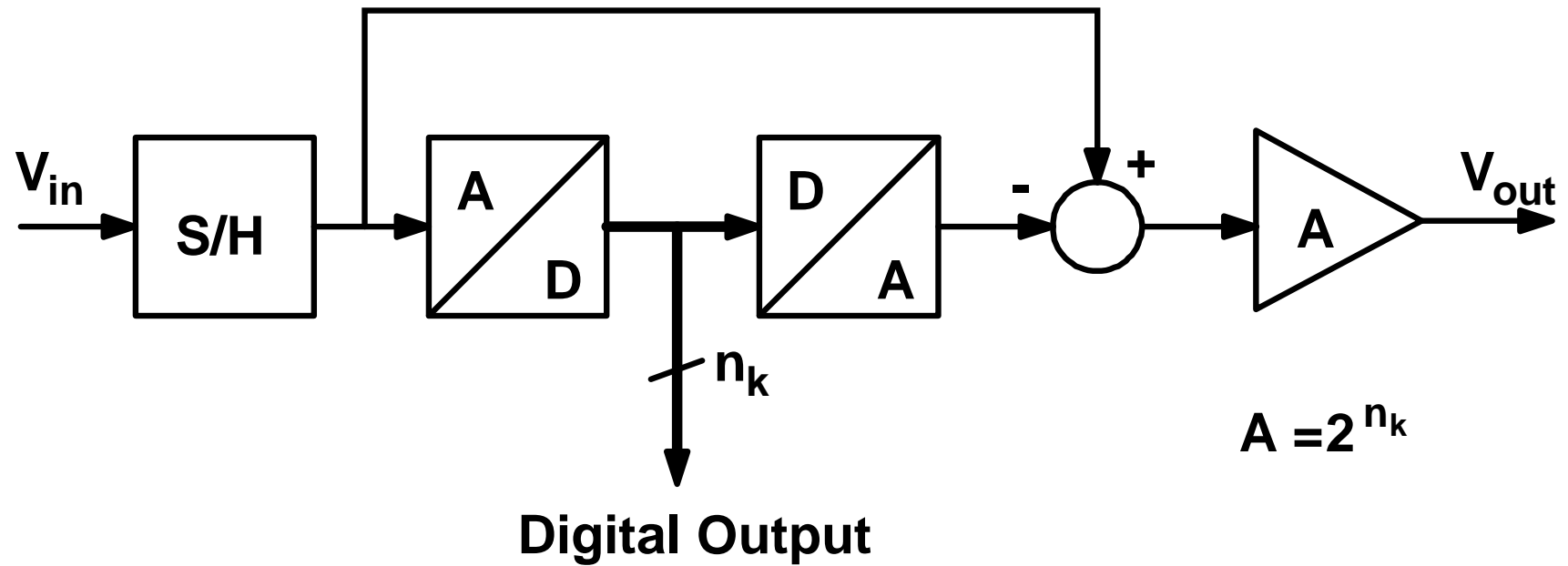
- [1] S. H. Lewis, P. R. Gray, 6/1987
- [2] I. Mehr, L. Singer, 3/2000
- [3] S. H. Lewis *et al*, 3/1992
- [4] I. E. Opris *et al*, 12/1998
- [5] D. W. Cline, P. R. Gray, 3/1996
- [6] S.-U. Kwak *et al*, 12/1997
- [7] M. K. Mayes, S. W. Chin, 12/1996

□ Journal of Solid-State Circuits, 1987 - 2000

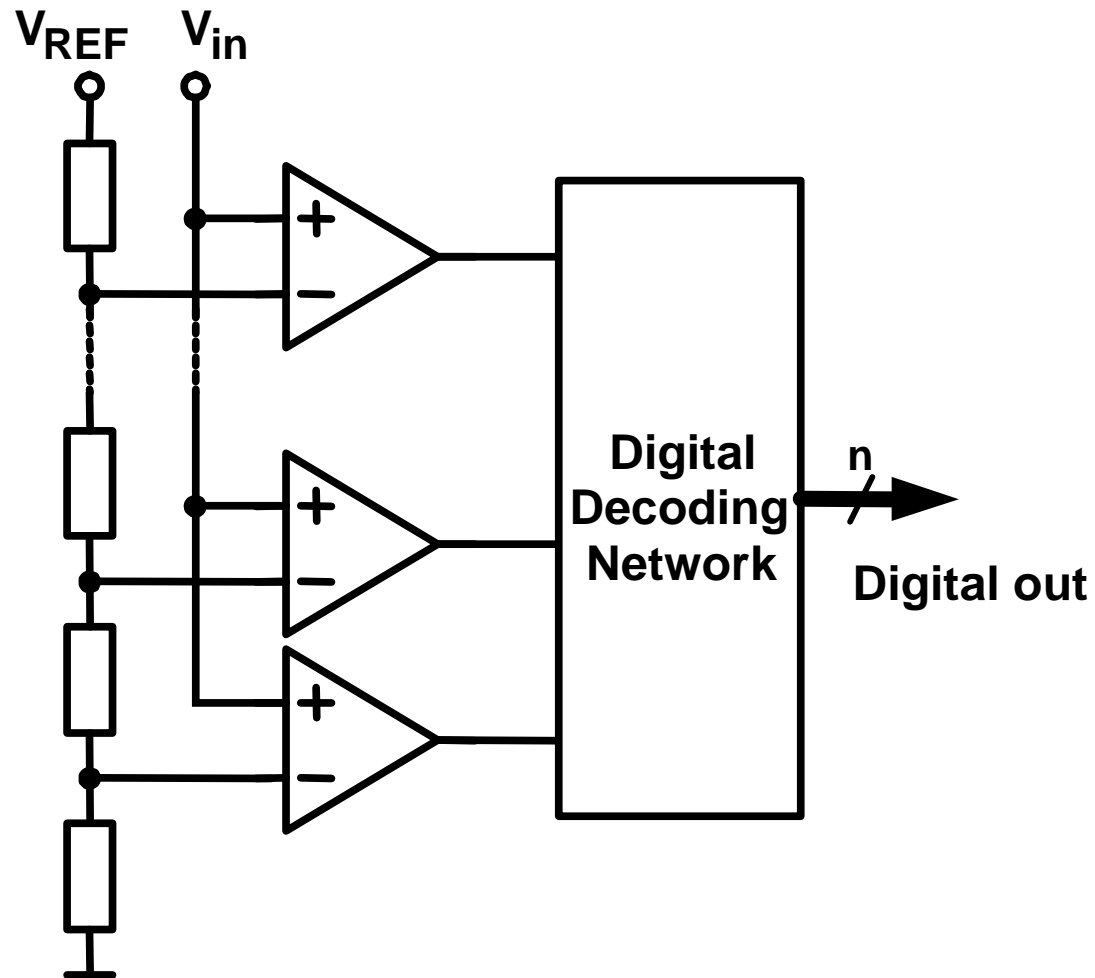
# Block Diagram



# One Pipeline Stage



# A/D Subconverter Implementation



Specifications:

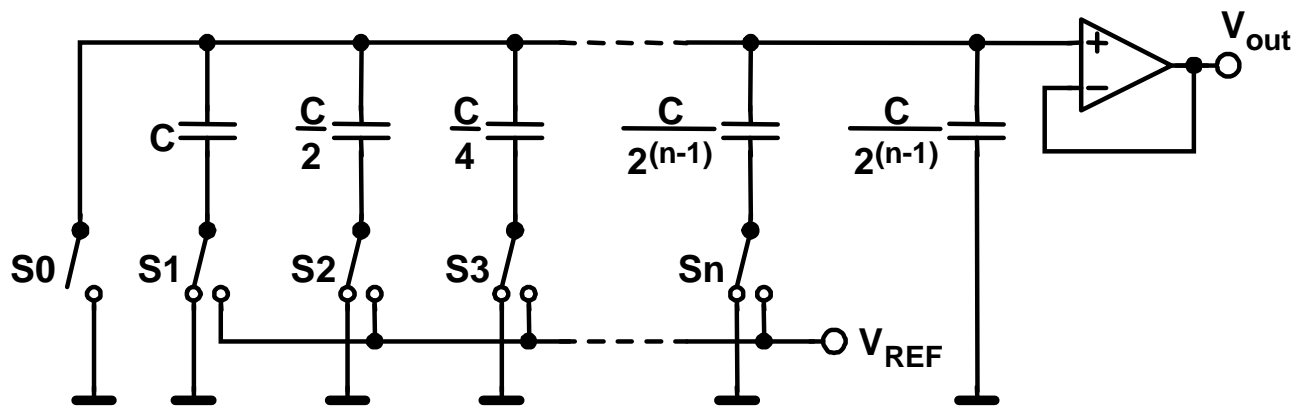
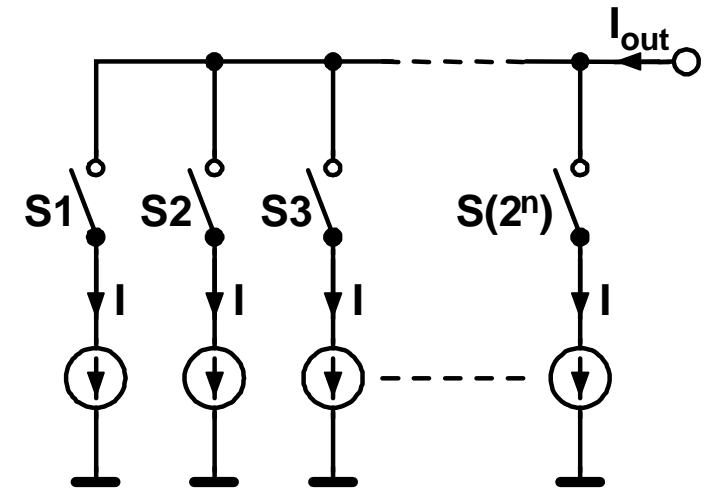
- High speed
- Low to moderate resolution

⇒ **Flash ADC**

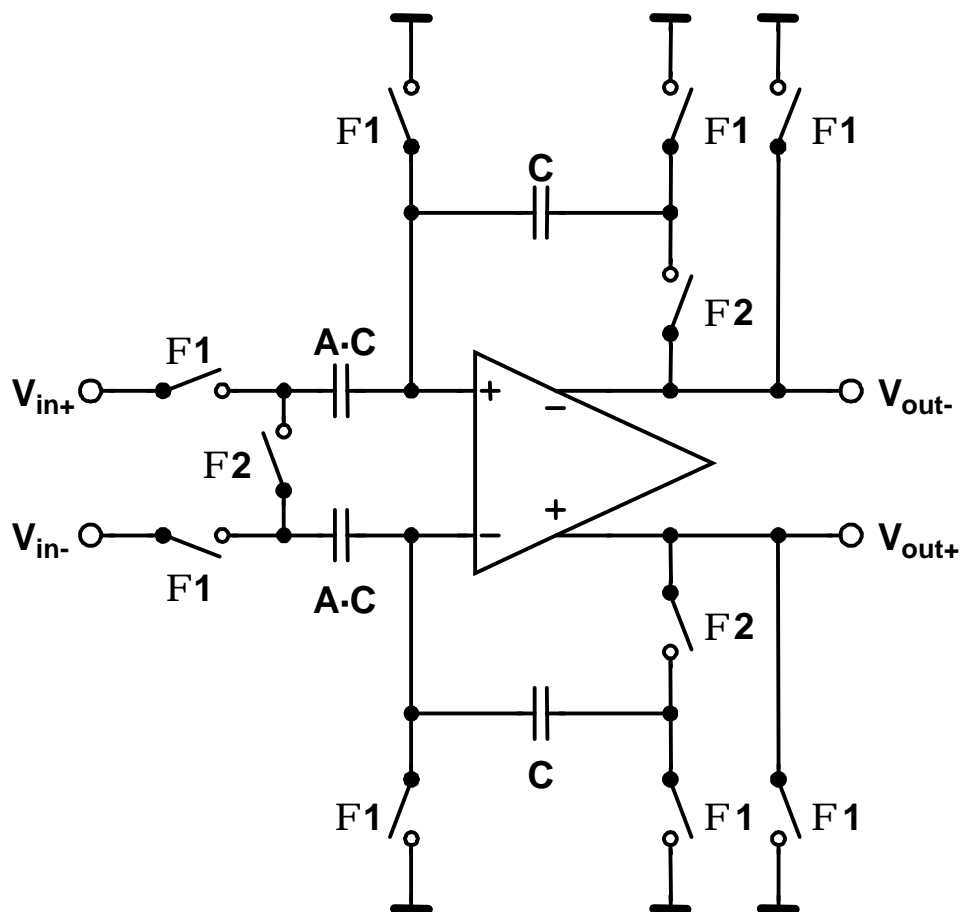
# D/A Converter Implementation

Widely used architectures in CMOS:

- ❑ Current-steering DAC
- ❑ Charge-scaling DAC

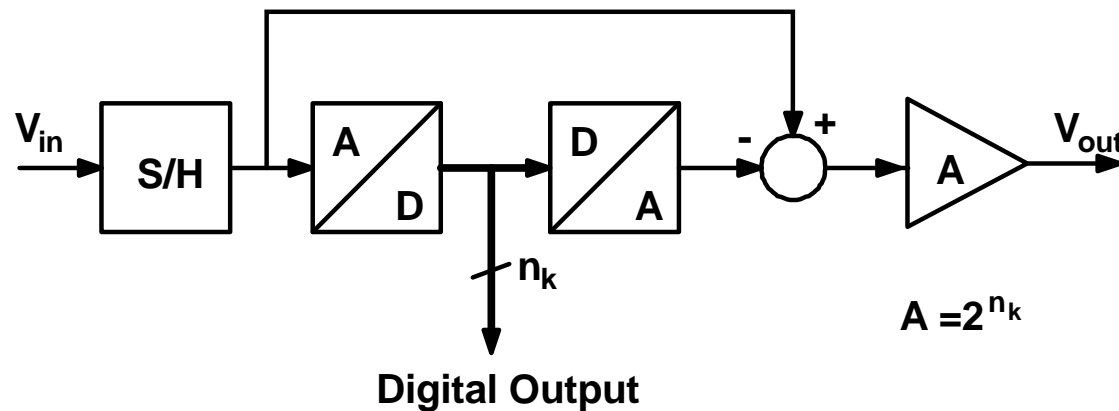


# S/H – Gain Stage Implementation



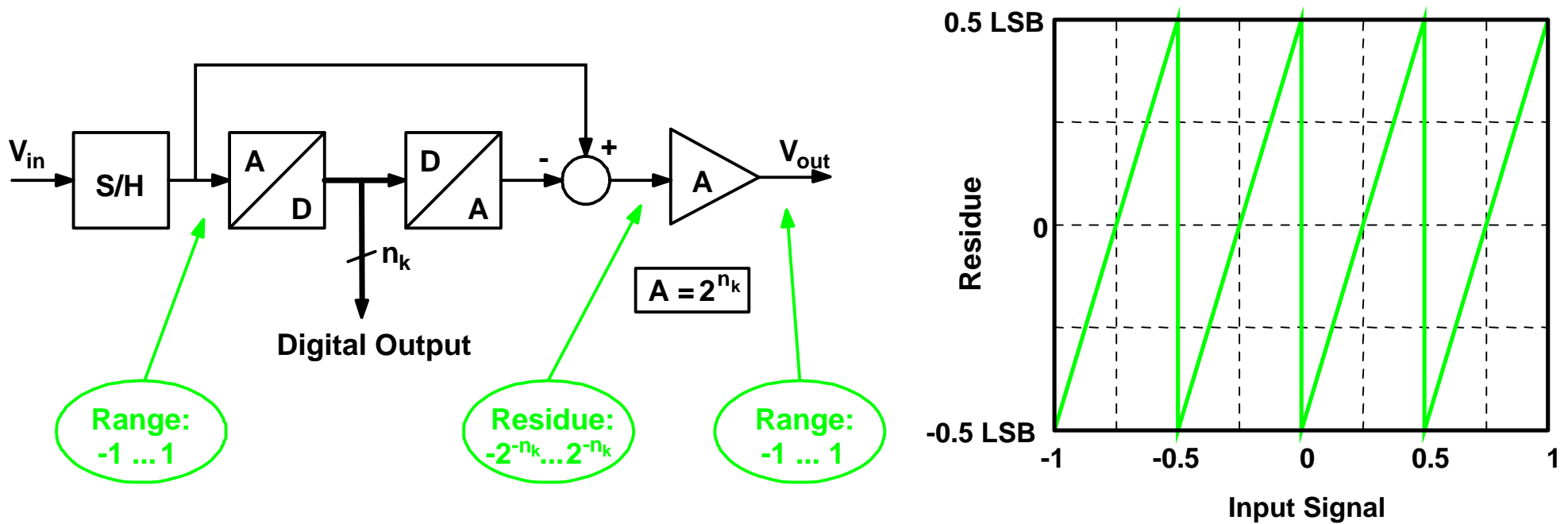
- ❑ S/H and gain stage normally combined into one building block
- ❑ Possible combination with charge-scaling DAC
- ❑ Scaling for different pipeline stages

# Errors Affecting Accuracy

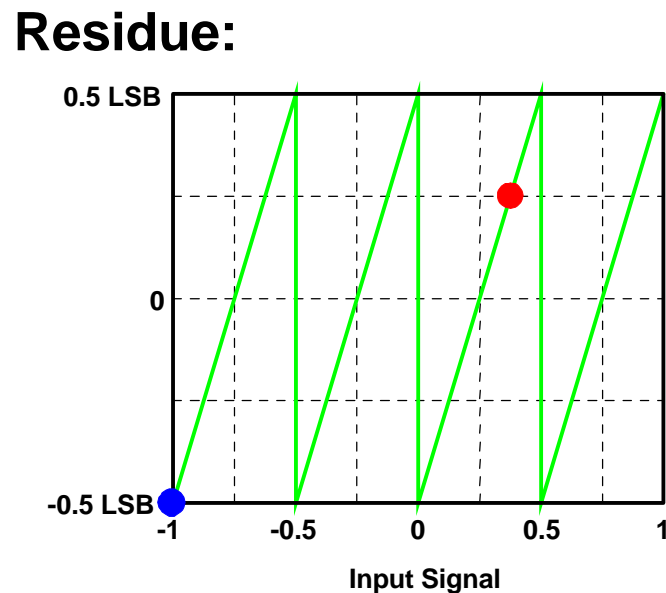
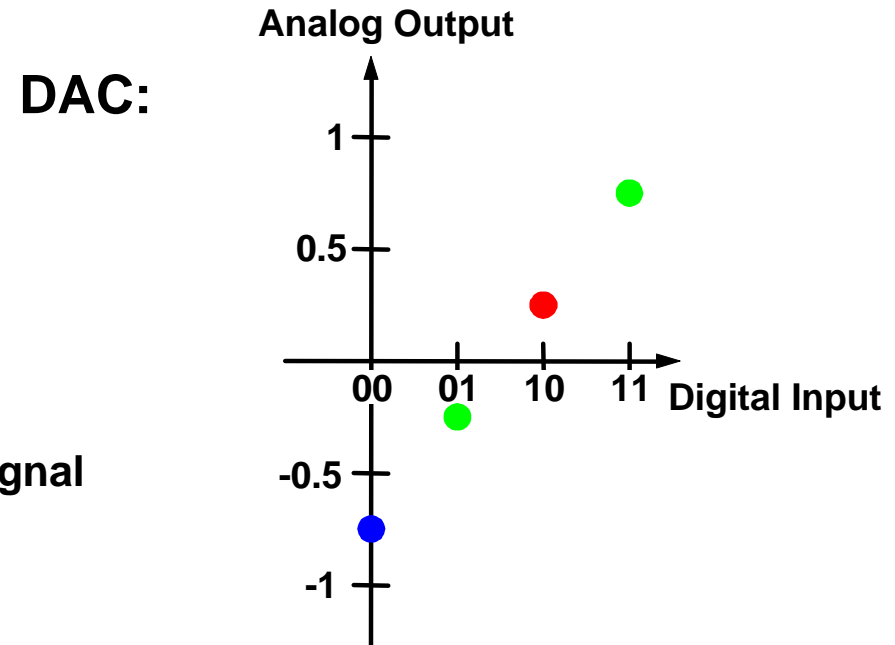
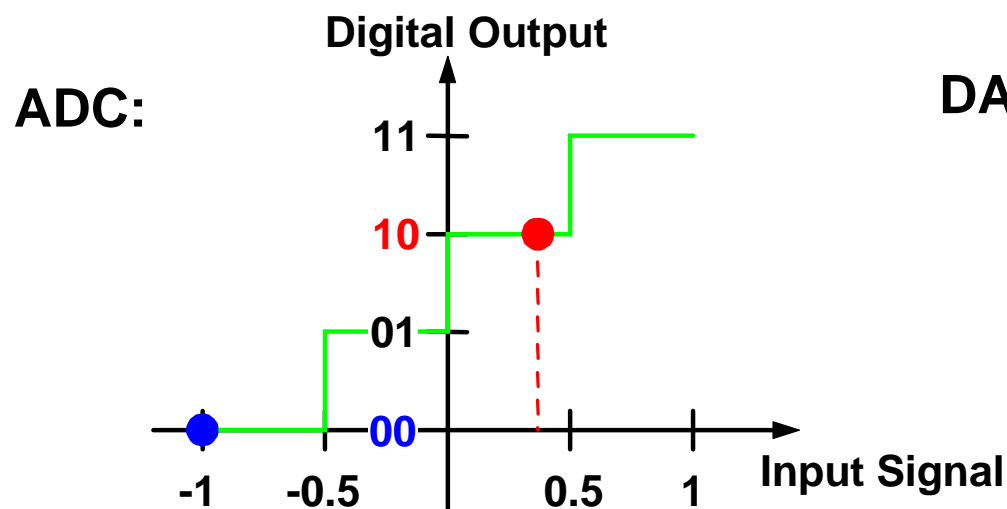


- ❑ Offsets
- ❑ Gain errors
- ❑ Non-linearity of A/D subconverter
- ❑ Non-linearity of D/A converter

# Residue and Digital Error Correction



# Details of Residue Mechanism



## Examples:

Analog input:  $-1 \Rightarrow$  ADC output: 00

$\Rightarrow$  DAC output:  $-0.75$

$\Rightarrow$  Residue:  $-0.25 = -0.5 \text{ LSB}$

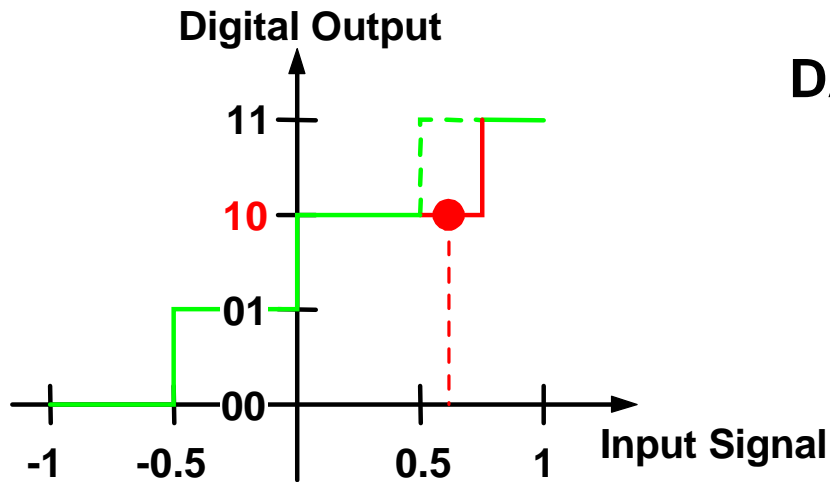
Analog input:  $0.375 \Rightarrow$  ADC output: 10

$\Rightarrow$  DAC output:  $0.25$

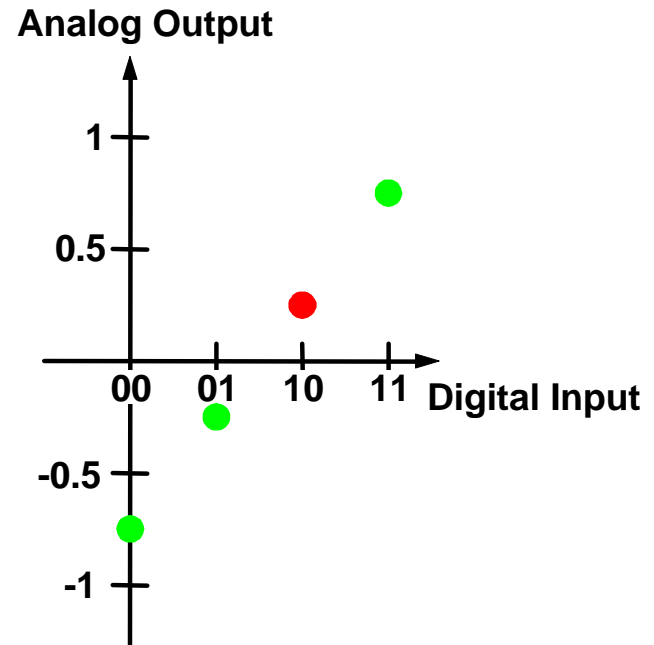
$\Rightarrow$  Residue:  $0.125 = 0.25 \text{ LSB}$

# Non-Linearity of the A/D Converter (I)

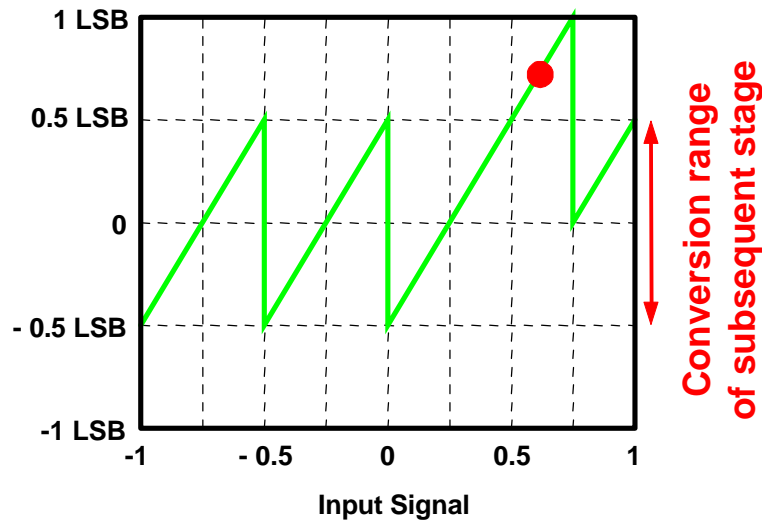
ADC:



DAC:



Residue:

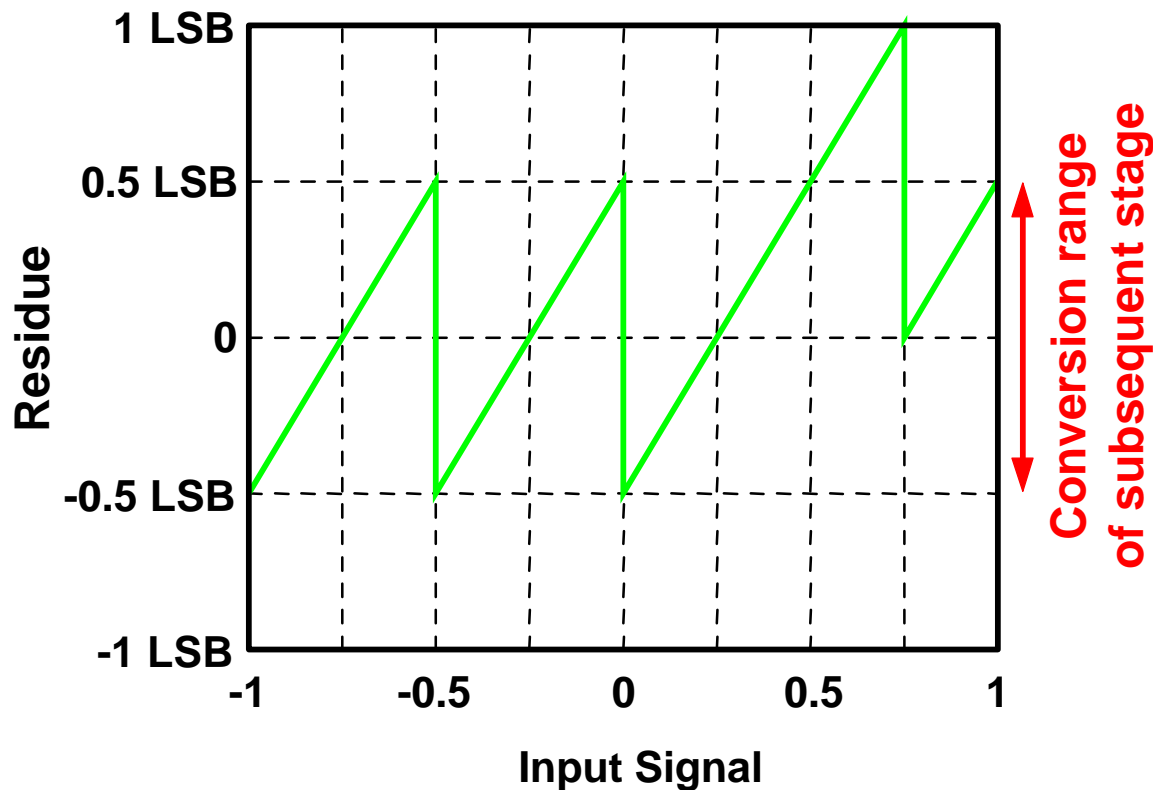


Example:

Error in the last A/D converter  
reference level:

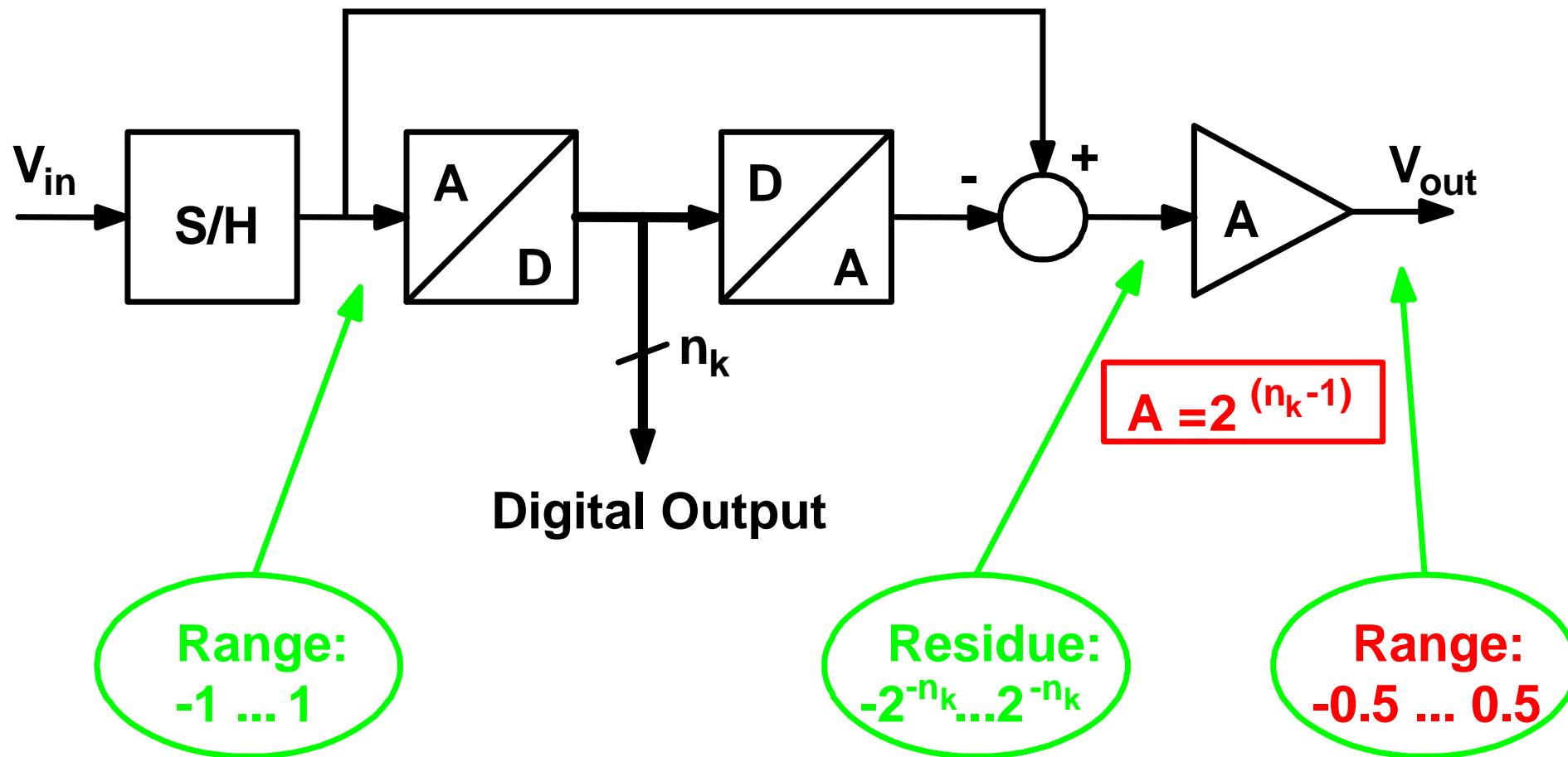
- ⇒ Analog input: 0.625
- ⇒ ADC output: 10 instead of 11
- ⇒ DAC output: 0.25
- ⇒ Residue: 0.375 = 0.75 LSB

# Non-Linearity of the A/D Converter (II)



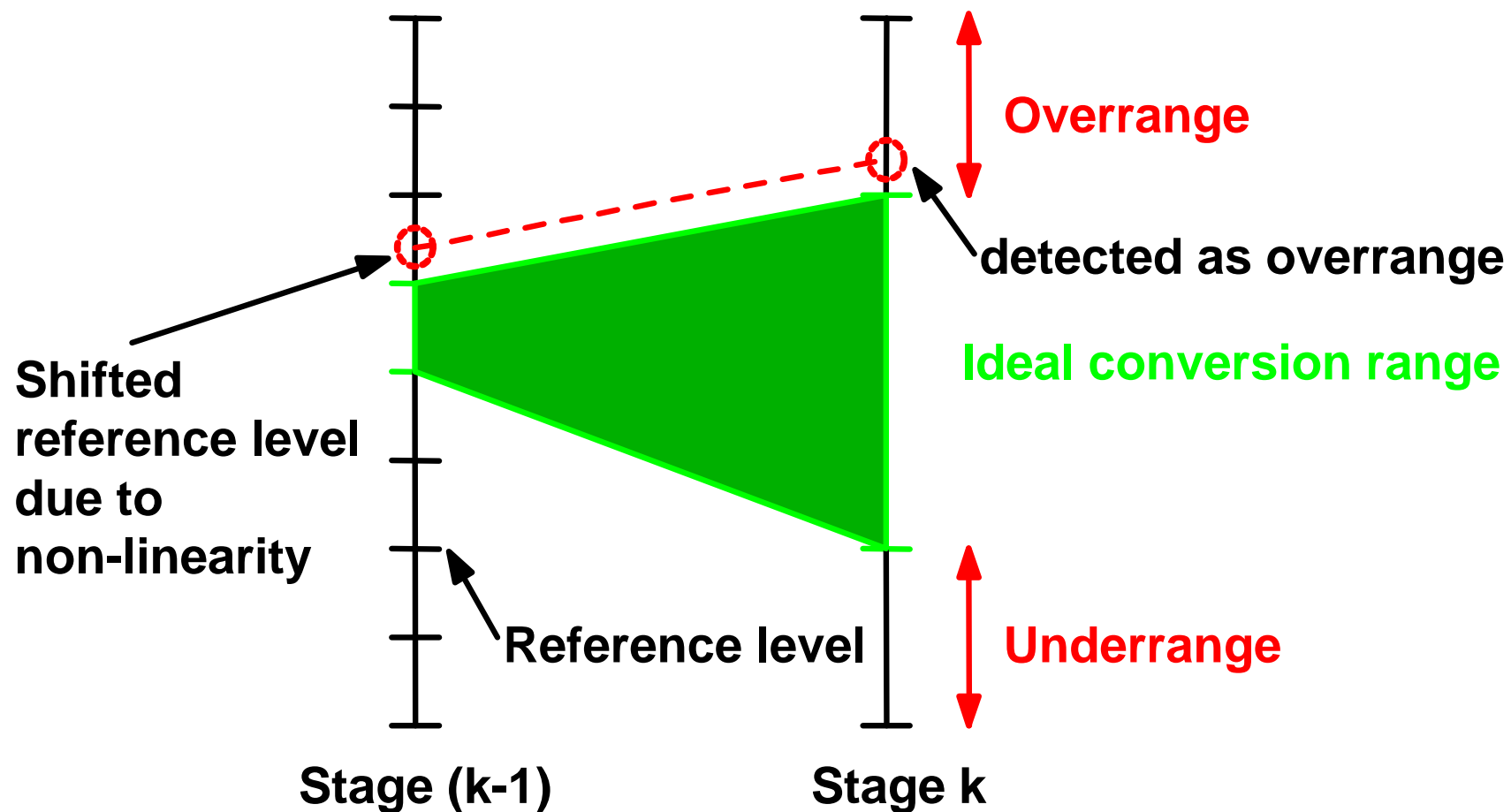
- ❑ Residue increases due to A/D converter error
- ❑ Subsequent stage cannot process the residue and clips it
- ❑ **But:** the residue contains the entire information of the signal

# First Step to Error Correction



- Gain reduction increases conversion range of the subsequent stage

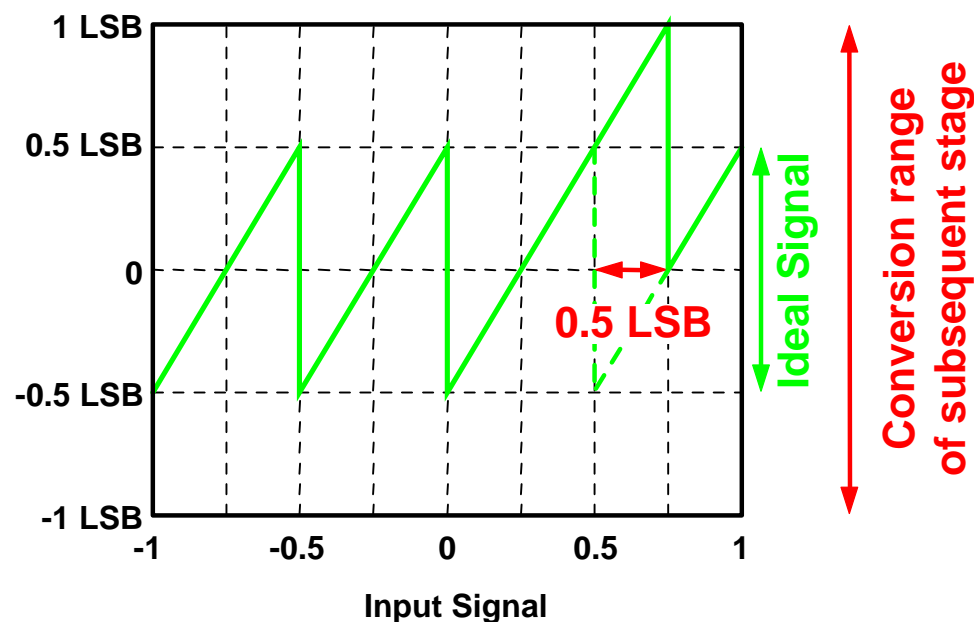
# Digital Error Correction (DEC)



# Errors That Can Be Corrected (I)

## □ A/D Subconverter non-linearity

- Shift of reference levels can be corrected
- As long as the residue is **within the conversion range** of the subsequent stage



## Example:

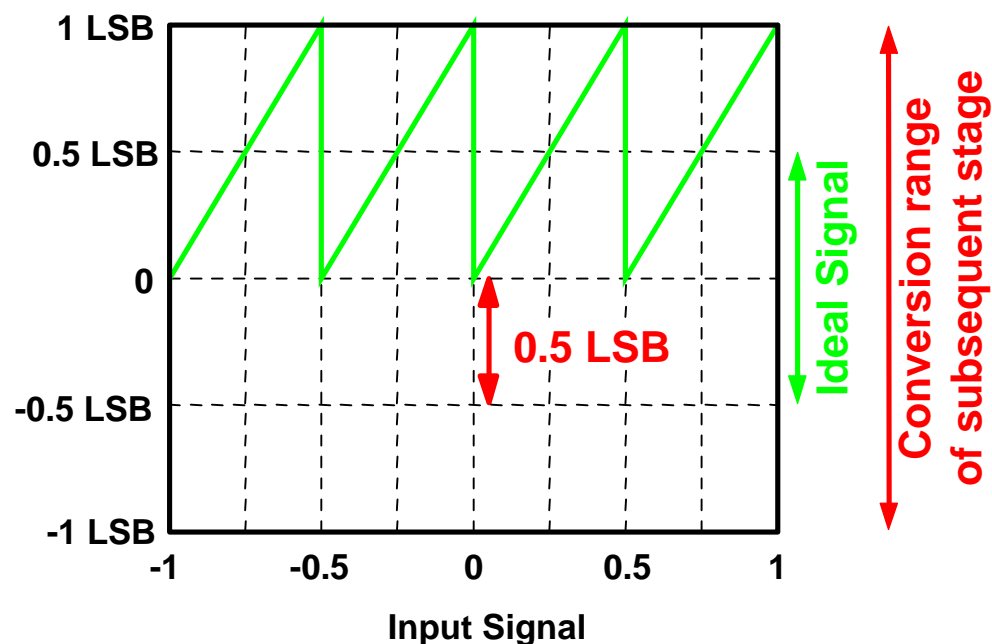
- One additional bit per stage for error correction
- Shift of reference level of  **$\pm 0.5$  LSB** can be corrected

# Errors That Can Be Corrected (II)

## □ Offset Errors of S/H and Interstage Amplifier

- Offset only shifts the residue

⇒ Same correction as for A/D Subconverter non-linearity



## Example:

- One additional bit per stage for error correction
- Offset of  $\pm 0.5$  LSB can be corrected
- For  $V_{FS} = \pm 1V$ , 2 bit/stage: correctable offset =  $\pm 250$  mV

# Errors That Cannot Be Corrected (I)

## □ D/A Converter non-linearity:

- **D/A Converter determines the accuracy of the entire pipelined A/D converter**
- **Accuracy of the residue depends on the accuracy of the D/A converter**
- **Accuracy of the D/A converter must be equal to the resolution of the entire A/D converter, not the stage resolution**

# Errors That Cannot Be Corrected (II)

## □ Interstage Gain error

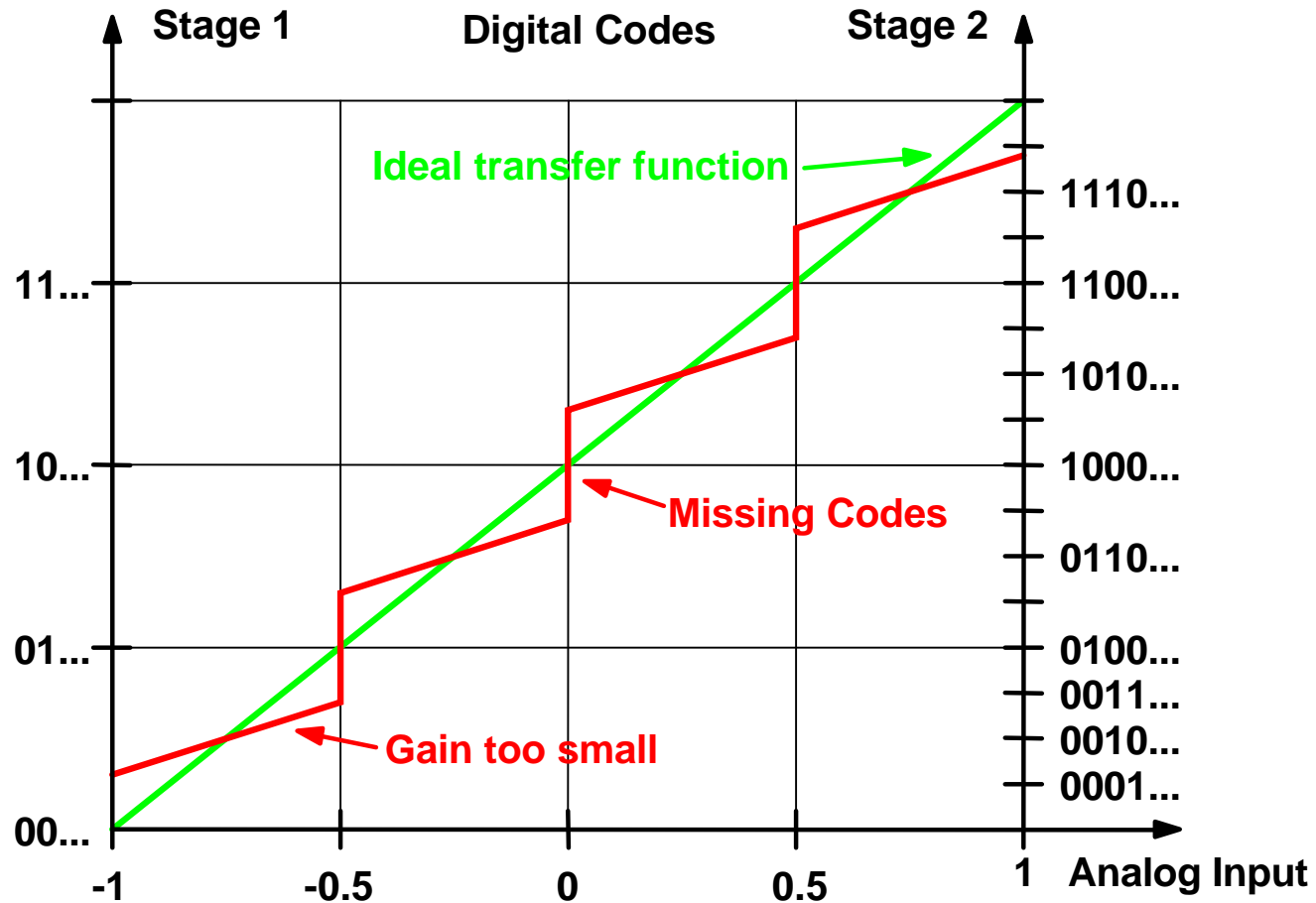
- does not affect residue = 0
- strongly affects large residues
- ⇒ **signal dependent error**
- must not compromise accuracy of subsequent stage

**Gain accuracy must be equal to the total resolution of the subsequent stages**

**Example: Converter with 14 bits, 2 bit per stage:  
Accuracy of first gain stage = 12 bit**

# Errors That Cannot Be Corrected (III)

## □ Interstage gain error (continued):



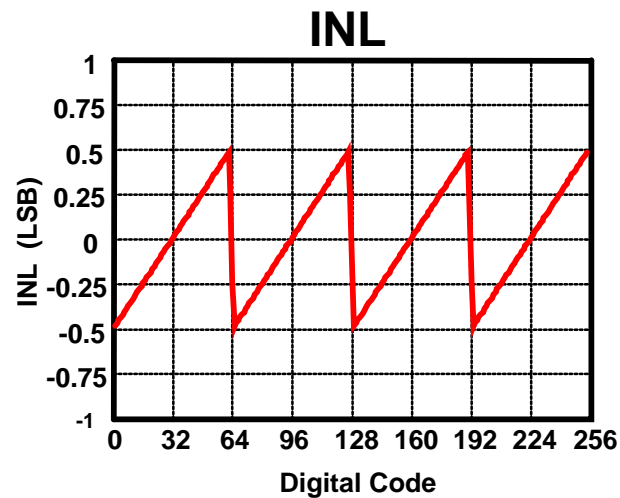
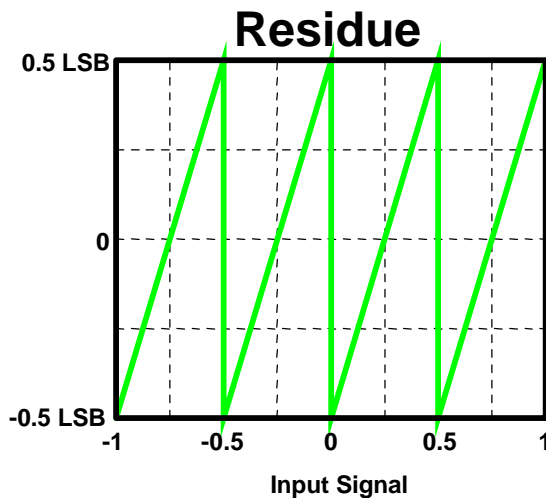
# Errors That Cannot Be Corrected (IV)

□ Interstage gain error (continued):

Gain:  $A = A_{id} (1 + ? A)$

- INL:  $INL_{max} = -(d-0.5) \text{ LSB}$  if  $DA = d \times 2^{-n_s}$
- DNL:  $DNL_{max} = (d-0.5) \text{ LSB}$  if  $DA = d \times 2^{-n_s}$

$n_s = \#$  bits of subsequent stages, no error correction

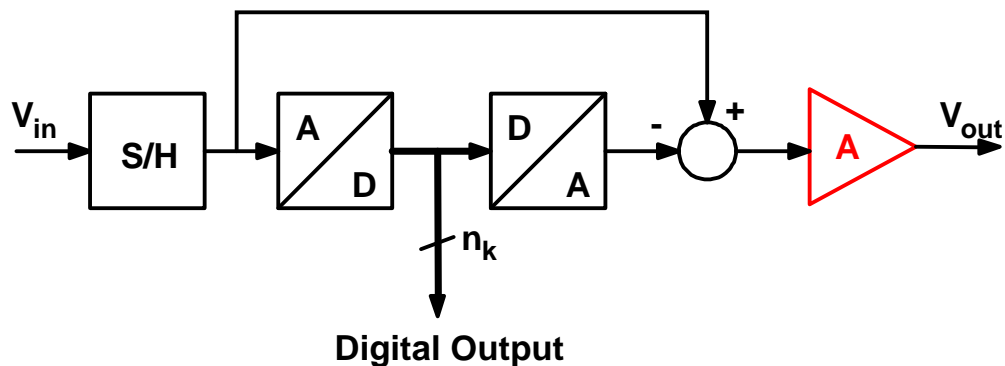


Numeric Example:

8 bit ADC, 2 bit/stage

Gain error after first stage: 1 LSB @ 6 bit

# Conversion Speed



- ❑ Limiting factor:  
interstage gain
- ❑ Maximum gain-bandwidth  
given by technology
- ⇒ Maximum speed for  
minimum gain
- ⇒ Stage resolution as low  
as possible

# Trade-Off Speed vs. Accuracy

## □ High conversion speed

⇒ low stage resolution

⇒ Often used: 1.5 bit/stage up to ca. 10 bit

## □ Gain Accuracy of first interstage gain

⇒ low stage resolution

- Matching accuracy of capacitors, resistors: ca. 10 bit

⇒ Stage resolution of 3...4 bit/stage for 13...14 bit ADC

## □ Other solution: calibration [1], error averaging [2] etc.

[1]: A. N. Karanicolas *et al*, JSSC Dec. 1993

[2]: B.-S. Song *et al*, JSSC Dec. 1988

# Noise

**Two main noise sources:**

□ **kT/C noise from input S/H**

⇒ **determines value of input sampling capacitance**

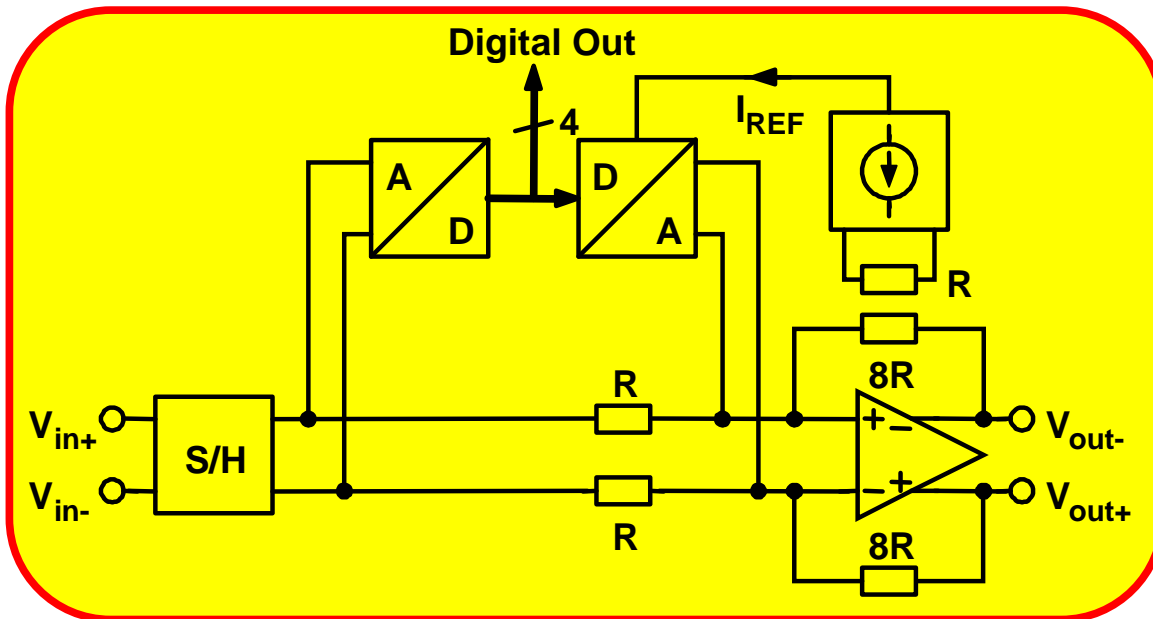
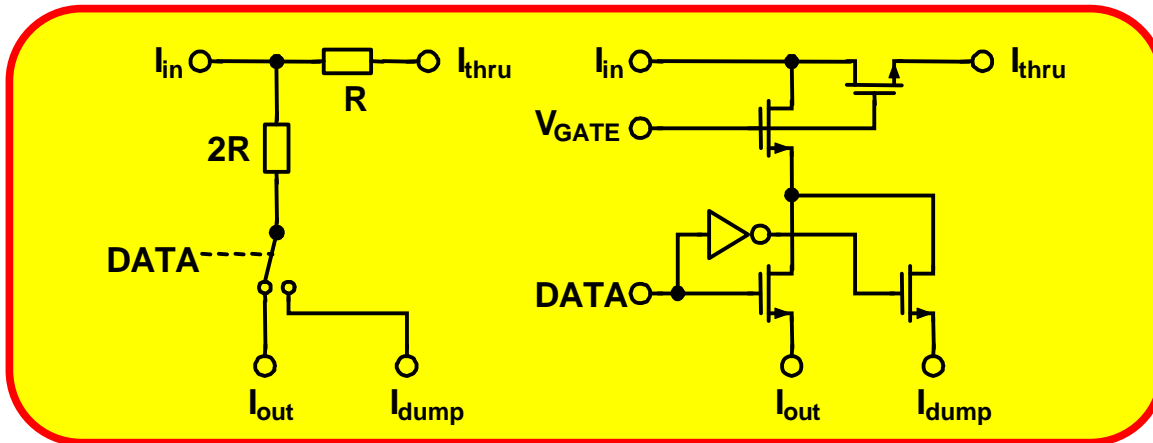
□ **Wide-band noise of D/A converter, reference and amplifiers**

⇒ **sampled by interstage S/H**

⇒ **contribution of subsequent stages reduced by gain**

⇒ **bandwidth of amplifiers only as high as necessary**

# A MOSFET-Only Pipelined A/D Converter



- ❑ MOSFET-only ladder
- ❑ No precise passive elements needed
- ❑ MOSFETs act as resistors
- ❑ High matching accuracy

0.25  $\mu\text{m}$  CMOS process

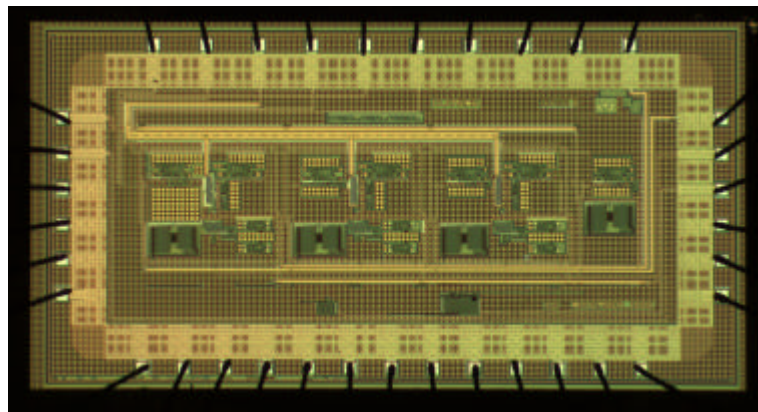
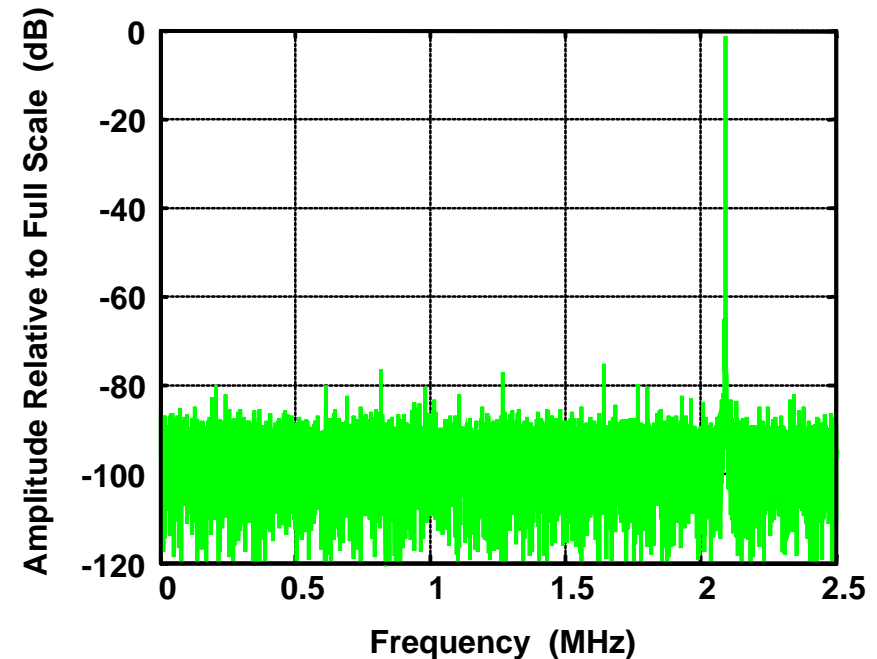
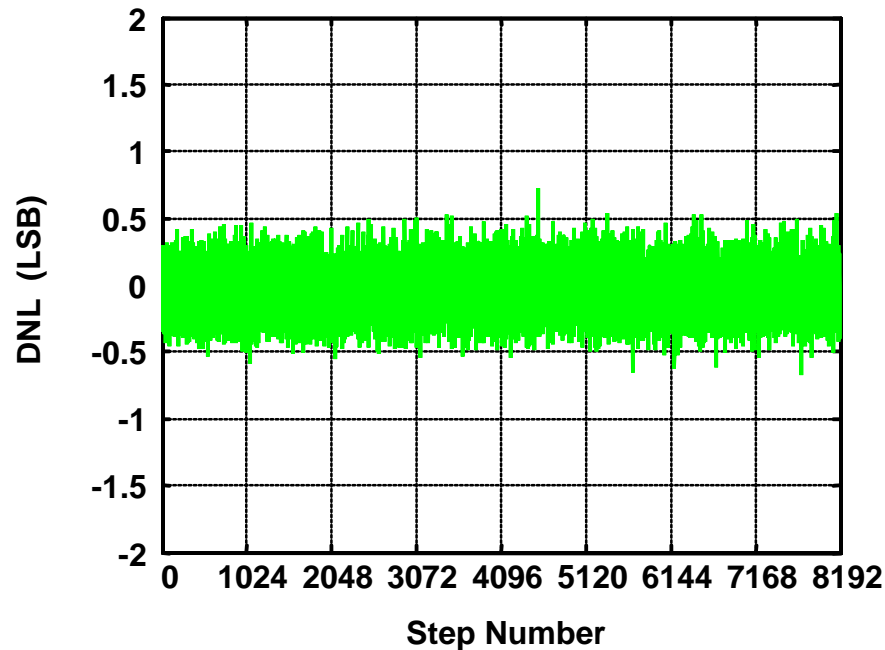
2.5 V supply

13 bit     4bit/stage

5 Msample/s

118 mW @ 2.5 V

# A MOSFET-Only Pipelined A/D Converter (II)



**Measurement:**

**Conversion Speed: 5 Msample/s**

**Input Signal: 2.09 MHz**