A Mismatch-Insensitive High-Accuracy High-Speed Continuous-Time Current Comparator in Low Voltage CMOS

R. del Río-Fernández, G. Liñán-Cembrano, R. Domínguez-Castro, and A. Rodríguez-Vázquez

Instituto de Microelectrónica de Sevilla - Centro Nacional de Microelectrónica
Avda. Reina Mercedes s/n, (Edif. CICA)
E-41012, Sevilla, Spain

Proc. Design of Circuits and Integrated Systems Conf. (DCIS’97)
pp. 139-144, Sevilla, November 1997
This paper presents a CMOS current comparator which employs nonlinear feedback to obtain high-accuracy (down to 1.5pA) and high-speed for low input currents (8ns@50nA). This structure is much faster for low currents (below 10µA) than other previous nonlinear feedback comparators [1], [2], [3], [4]. Particularly, when compared to the fastest current comparator reported up to now [4], the new one goes more than 100 times faster for 1nA current, with smaller area occupation and similar power consumption. In addition, the new comparator is virtually insensitive to mismatch and capable to operate with supply voltages as low as 1V.

1. Introduction

Analog current-mode techniques are drawing strong attention today due to their potential application in the design of high-speed mixed-signal processing circuits in low voltage standard VLSI CMOS technologies [5]. Also current-mode circuits are natural candidates for image sensory information processing where current sensing and comparison is necessary. Current comparators are basic building blocks for nonlinear current-mode signal processing and analog to digital converters. The availability of large current ranges is an appealing feature for both fields. Also, efficient small current level detection is fundamental for high accuracy and high speed applications.

Low level, high speed current detection is also required in different light and radiation sensing applications: i.e. γ-detectors using wide band gap semiconductors [6], or controllability and reconfigurability issues in E-beam testing of integrated circuits [7]. For instance, in the latter the need arises to detect current levels as low as 1nA in a few µs. Subthreshold CMOS current mode massive computation architectures [8] also require efficient detection of low current levels for fast discriminating function evaluation. To highlight another application, current detection is also required in IDDQ VLSI testing approaches [9].

In recent years, many current comparator circuits have been proposed [1], [2], [3], [4], [10], [11], [12]. A possible classification of them is to distinguish between the ones where the input current is first sensed at a low impedance node (resistive input) and then amplified using a voltage gain mechanism, and the ones where the input current is sensed at a high impedance node (capacitive input). The firsts provide high speed for high current levels but are somewhat inaccurate; the seconds obtain enlarged resolution at the cost of increasing voltage excursions at the input node and consequently decreasing the operation speed [12].

Another possible classification is to distinguish between the structures that use autozeroing techniques to attenuate offset or to reduce propagation delays by adding clock signal generation circuitry and the ones that work on asynchronous mode.

In this paper we propose an asynchronous mode current comparator that uses nonlinear feedback to combine the advantages of capacitive-input and resistive-input architectures. Because the proposed circuit is offset insensitive by construction it does not require autozero for offset attenuation. We include also a comparative study with the operation of the current comparator which is claimed the fastest among all
2. Circuit behaviour

2.1. The Current Switch Comparator

Fig.1 shows the schematic of the so-called Current Switch Comparator, whose advantages for low input currents have been demonstrated in [12]. The operation of this circuit involves two different regions.

If a positive current flows towards the input node, and assuming null initial conditions ($V_{in} = V_o = E$) transistors $M_n$ and $M_p$ are OFF, therefore the equivalent impedance at the input node is capacitive and consequently the circuit exhibits a very high resolution (only limited by the leakage currents); the input current is integrated in the parasitic input capacitor ($C_{in}$) producing a continuous increase of the input voltage. The amplifier causes $V_o$ to decrease faster than $V_{in}$ and so that $M_p$ turn ON draining the input current and closing a negative feedback loop around the amplifier. It obtains a virtual ground at the amplifier input, thus fixing the voltage at the input node. A similar situation occurs for negative input current where $M_n$ becomes ON.

The transient evolution is dominated by the first operation mode (the capacitive input behaviour), and if we consider a single pole model for the amplifiers with a gain-bandwidth product ($GB$) and linear capacitors for their input and output nodes one obtains

$$\Delta V_{in} = \frac{I_{in}}{C_{in}}$$

$$\Delta V_o = \frac{GB}{2} \frac{I_{in}^2}{C_{in}}$$

(1)

However, due to the parasitic capacitors between input and output nodes ($C_M$) the transient response is slowed down even for an ideal amplifier; this behaviour is similar to the slew rate phenomena in Miller operational amplifiers. In the comparator of Fig.1 the coupling capacitor is formed by the $C_{gs}$ capacitors of $M_n$ and $M_p$, and eventually the intrinsical coupling capacitor of the amplifier. Due to $C_M$, input and output nodes of the comparator are coupled, so that the transient response evolution follows a linear characteristic instead a quadratic law

$$\Delta V_{in} = \frac{(C_o + C_M)}{C^2} I_{in} t$$

$$\Delta V_o = \frac{C_M}{C^2} I_{in} t$$

(2)

where $C^2 = C_{in} C_o + C_{in} C_M + C_o C_M$.

Note that in (1) the output voltage is directly proportional to the amplifier $GB$, and hence the faster the amplifier is the faster the current comparator solves. However in (2) this dependence is vanished.

The response time can be calculated from (1) and (2) by making $\Delta V_o(T_D) = E_{OH}$, where $E_{OH}$ denotes the logic noise margin.

$$T_D = \frac{C^2 E_{OH}}{C_M \frac{I_{in}}{C_{in}}} : (C_M \neq 0)$$

$$T_D = \frac{2C_{in} E_{OH}}{GB \frac{I_{in}}{C_{in}}} : (C_M = 0)$$

(3)

According to these formula, Fig.2 shows a comparison of the response time for the current switch comparator of Fig.1 with and without the coupling capacitor. We are assuming $E_{OH}$=1V, typical capacitances values of $C_{in}$=$C_o$=50fF and $g_m$=100µA/V for the amplifier.

![Fig. 1 Current Switch Comparator Schematic.](image1)

![Fig. 2 Time response comparison for the current comparator with and without coupling capacitor.](image2)
For low current levels, it is seen that the comparator behaviour becomes severely degraded due to the coupling capacitor, even for low values of this capacitor. On the other hand, for large currents (in the order of tens of µA) smaller times response are obtained in the coupled current comparator. For these high current levels a simple inverter features fast operation speed, with no feedback needed.

2.2. The New Structure

To improve transient response of the current switch comparator for low input currents, circuit strategies are required to uncouple input and output nodes of the amplifier and hence, reducing the coupling capacitance.

In order to achieve faster response times simple CMOS inverters are usually used as amplifiers. To avoid the overlap capacitors influence cascode transistors could be used in the amplifier output node. Also, the feedback mechanism used to obtain the nonlinear driving-point characteristic should be modified to avoid $M_p$ and $M_n C_{gs}$ influence, so that using a source follower in the feedback loop must be avoided.

The new comparator schematic is shown in Fig.3. The circuit has two operation zones. If a positive current flows towards the input node, and assuming that the initial conditions are:

$$V_{in} = V_o = E \quad V_n \leq E + V_{tn} \quad V_p \geq E - |V_{tp}| \quad (4)$$

transistors $M_n$ and $M_p$ are OFF, so that the equivalent impedance at the input node is capacitive (i.e., very large in DC) and consequently the circuits exhibits a very high resolution (only limited by the leakage currents); the input current is integrated in the input capacitor ($C_{in}$) and produce a continuous increase of the input voltage. The amplifier causes $V_o$ to decrease faster than $V_{in}$, increasing $V_{gs}$ for the transistor $M_n$ and decreasing $V_{gs}$ for $M_p$, so that $M_n$ is driven into the ON state and a negative feedback loop is created around the amplifier. It obtains virtual ground at the amplifier input, fixing the voltage at the input node. A similar situation occurs for negative currents, where $M_p$ becomes ON.

This structure reduces response times of the Fig.1 comparator. An improvement around two orders of magnitude is observed with the comparator in [4] if we compare the worst cases (negative input currents).

We can also obtain a symbolic expression for the response time by transient analysis. If we consider an input current step at $t=0$ from a negative overdrive level $-J$ up to a positive overdrive level $+J$, the response time can be written as follows:

$$T_p \equiv \frac{2C_{in} (V_p - V_n + V_{tn} + |V_{tp}|)}{GB J} \quad (5)$$

Fig.4 shows the final schematic for the new current steering comparator. As it can be seen the amplifier that appears in Fig.3 has been implemented by a CMOS inverter with two cascode transistors which avoid the capacitors between input and output nodes, so that the transient evolution presents a quadratic time dependence instead of a linear dependence, as
The response times simulation measures of the two comparators for a range of input currents are shown in Fig. 5. We have considered the worst case, i.e. a step input current from a positive overdrive level \( +J \) to a negative overdrive level \( -J \). The results show that the greatest speed improvement occurs for low input currents, and for less than 10\( \mu \)A the new comparator remains faster than the one in [4]. The quadratic time law predicted in (2) can be observed in Fig. 6. It can be seen how this approach is suitable in order to describe the main transient evolution. It contrasts with the behaviour observed in Fig. 7 where the slewrate phenomena governs the temporal response. The circuit which provides the waveform in Fig. 7 is the same as in Fig. 4 but using the feedback scheme that appears in Fig. 1.

A possible technique to improve comparison times is to reduce the voltage excursions at the amplifier output node. This approach was applied by the authors in [4] to the circuit in Fig. 1. However it presents a very high sensitivity to mismatch effects. In order to avoid the mismatch influence the excursions on the output voltage must be larger than the expected maximum fluctuations due to mismatch.

Fig. 8 shows a comparative study by Monte Carlo analysis of the new and [4] comparators designed in the same technology (CMOS 1.6\( \mu \)m). It is shown how the percentage of successful comparisons for [4] decreases as input current level becomes lower. However, for the new comparator this percentage becomes 100\% as soon as the input current reaches the maximum offset level (<1.5pA).

2.3. Simulation Results

A prototype of the comparator has been designed in a CMOS 0.7\( \mu \)m technology. Fig. 9 illustrates the associated layout, including the biasing circuitry. Die size, without bounding pads, is 62 \( \mu \)m x 80 \( \mu \)m.
The main features of this prototype for a 5V voltage supply are:

- Input Current Offset lower than 1.2pA.
- Maximum resolution in the order of few pA.
- Maximum delay for a 50nA step input current: 11ns.
- Maximum delay for a 1µA step input current: 2ns.
- Power consumption: 2.5mW.

Fig.10 shows the response time measured from the extracted netlist for different input currents. As it can be seen, the basic dependence showed in Fig.5 still remains in the presence of parasitics. Obviously, the response time degrades due to the layout parasitics. However, even considering these parasitics, the new comparator operates much faster than the one in [4]. On the other hand, the accuracy feature remains unchanged in the presence of layout parasitics.

Another important feature of this new structure is its capability for working at low voltage supplies. As it can be seen in Fig.4 the biasing circuitry requires

\[ V_{DD} > 2V_{in} + |V_{th}| \]

whereas the CMOS amplifier needs

\[ V_{DD} > V_{in} + |V_{th}| + 2V_{dsat} \]  \hspace{1cm} (7)

It allows proper operation with a power supply below 3V. If a lower power supply is needed the biasing circuitry should be modified, in this case (7) provides the minimum \( V_{DD} \) value (lower than 2V). This comparator can operate even below this limit if the amplifier in Fig.11 is used. In this case the new limit becomes around 1V.

\[ V_{DD} > \frac{V_{in}}{3V_{dsat}} \]  \hspace{1cm} (8)

Fig.12 shows the response times of the comparator in Fig.4 for two different rail-to-rail voltages. It can be observed how for low input current levels the maximum speed is obtained using a 3.3V rail-to-rail voltage. It is due to lower voltage excursions at the output node of the amplifier.

3. Conclusions

An analysis of the transient evolution of nonlinear feedback current comparators demonstrates that its response time degrades significantly at low currents.
due to the influence of a Miller coupling capacitor. This can be partially overcome by reducing the voltage excursions; the price to be paid for this is a reduction of the circuit tolerance to mismatches, specially significant at low-voltage supplies. The comparator presented in this paper uses another strategy to obtain large operation speed without degrading the comparator resolution and keeping the comparator operation virtually mismatch-insensitive, even for voltage supplies as low as 1V.

Acknowledgment: This work has been funded by Spanish CICYT under contract TIC96-1392-C02-02 (SIVA: Active Vision Integrated System).

References:


